ANALOG-DIGITAL CONVERSION

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CHAPTER 7
DATA CONVERTER SUPPORT CIRCUITS

SECTION 7.1: VOLTAGE REFERENCES

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Reference circuits and linear regulators actually have much in common. In fact, the latter could be functionally described as a reference circuit, but with greater current (or power) output. Accordingly, almost all of the specifications of the two circuit types have great commonality (even though the performance of references is usually tighter with regard to drift, accuracy, etc.). This section discusses voltage references, and the next section covers linear regulators, with emphasis on their low dropout operation for highest power efficiency.

Precision Voltage References

Voltage references have a major impact on the performance and accuracy of analog systems. A ±5-mV tolerance on a 5-V reference corresponds to ±0.1% absolute accuracy—only 10 bits. For a 12-bit system, choosing a reference that has a ±1-mV tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. Note that many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be. Figure 7.1 summarizes some key points of the reference selection process.

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen for temperature coefficient and aging characteristics which preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up, and their behavior with transient loads. With regard to the first, always bear in mind that voltage references *do not power up instantly* (this is true of references inside ADCs and DACs as well as discrete designs). Thus it is rarely possible to turn on an ADC and reference, whether internal or external, make a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving.

Regarding the second point, a given reference IC may or may not be well suited for pulse-loading conditions, dependent upon the specific architecture. Many references use low power, and therefore low bandwidth, output buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs (especially successive approximation and flash ADCs). Suitable decoupling can ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer amplifier may be used to drive the node where the transients occur.

References, like almost all other ICs today, are fast migrating to such smaller packages such as SO-8 and MSOP, and the even more tiny SOT-23 and SC-70, enabling much higher circuit densities within a given area of real estate. In addition to the system size reductions these steps bring, there are also tangible reductions in standby power and cost with the smaller and less expense ICs.

- **Tight Tolerance Improves Accuracy, Reduces System Costs**
- **Temperature Drift Affects Accuracy**
- **Long-Term Stability, Low Hysteresis Assures Repeatability**
- **Noise Limits System Resolution**
- **Dynamic Loading Can Cause Errors**
- **Power Consumption is Critical to Battery Systems**
- **Tiny Low Cost Packages Increase Circuit Density**

Figure 7.1: *Choosing Voltage References for High Performance Systems*

Types of Voltage References

In terms of the functionality of their circuit connection, standard reference ICs are often only available in *series*, or *three-terminal* form (V_{IN}, Common, V_{OUT}), and also in positive polarity only. The series types have the potential advantages of lower and more stable quiescent current, standard pre-trimmed output voltages, and relatively high output current without accuracy loss. *Shunt*, or *two-terminal* (i.e., diode-like) references are more flexible regarding operating polarity, but they are also more restrictive as to loading. They can in fact eat up excessive power with widely varying resistor-fed voltage inputs. Also, they sometimes come in non-standard voltages. All of these various factors tend to govern when one functional type is preferred over the other.

Some simple diode-based references are shown in Figure 7.2. In the first of these, a current driven forward biased diode (or diode-connected transistor) produces a voltage, $V_f = V_{REF}$. While the junction drop is somewhat decoupled from the raw supply, it has numerous deficiencies as a reference. Among them are a strong TC of about –0.3%/°C, some sensitivity to loading, and a rather inflexible output voltage: it is only available in 600-mV jumps.

By contrast, these most simple references (as well as all other shunt-type regulators) have a basic advantage, which is the fact that the polarity is readily reversible by flipping connections and reversing the drive current. However, a basic limitation of all shunt regulators is that load current must always be less (usually appreciably less) than the driving current, I_D.

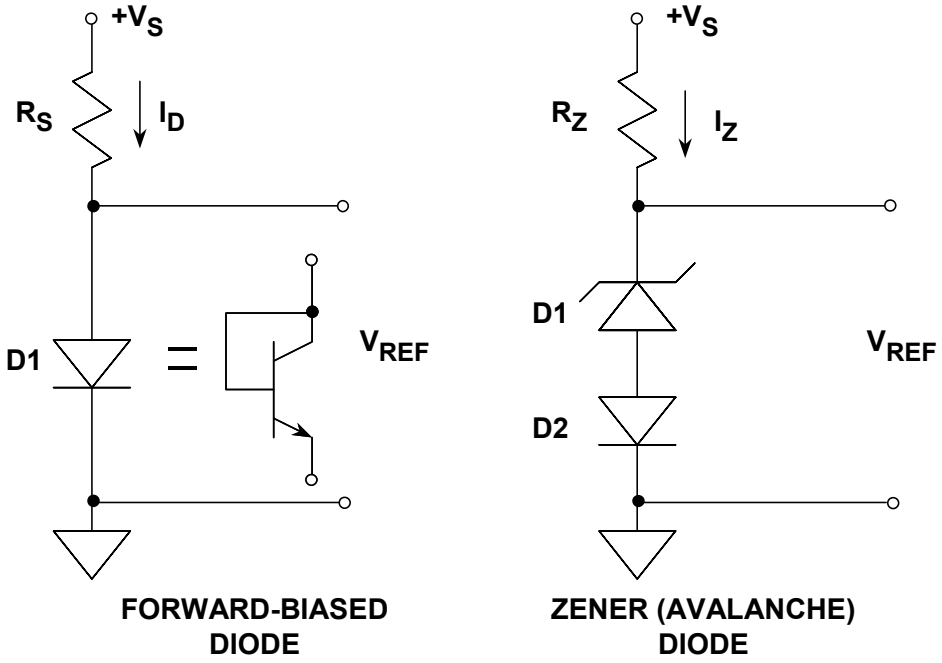


Figure 7.2: *Simple Diode Reference Circuits*

In the second circuit of Figure 7.2, a Zener or avalanche diode is used, and an appreciably higher output voltage realized. While true *Zener* breakdown occurs below 5 V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. Note that diode reverse breakdown is referred to almost universally today as *Zener*, even though it is usually avalanche breakdown. With a D1 breakdown voltage in the 5- to 8-V range, the net positive TC is such that it equals the negative TC of forward-biased diode D2, yielding a net TC of 100 ppm/°C or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package "temperature-compensated Zener" references, such as the 1N821-1N829 series.

The temperature-compensated Zener reference is limited in terms of initial accuracy, since the best TC combinations fall at odd voltages, such as the 1N829's 6.2 V. And, the scheme is also limited for loading, since for best TC the diode current must be carefully controlled. Unlike a fundamentally lower voltage (<2 V) reference, Zener diode based references must of necessity be driven from voltage sources appreciably higher than 6-V levels, so this precludes operation of Zener references from 5-V system supplies. References based on low TC Zener (avalanche) diodes also tend to be noisy, due to the basic noise of the breakdown mechanism. This has been improved greatly with *monolithic* Zener types, as is described further below.

At this point, we know that a reference circuit can be functionally arranged into either a series or shunt operated form, and the technology within may use either bandgap based or

Zener diode based circuitry. In practice there are all permutations of these available, as well as a third major technology category. The three major reference technologies are now described in more detail.

Bandgap References

The development of low voltage (<5 V) references based on the bandgap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first of these was the LM109 (Reference 1), and a basic bandgap reference cell is shown in Figure 7.3.

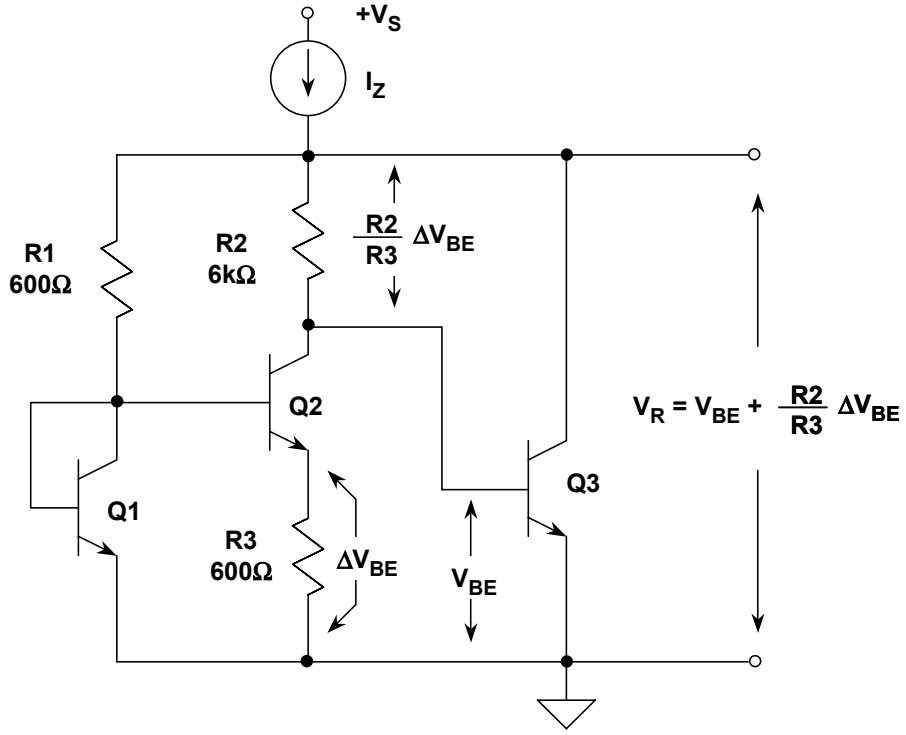


Figure 7.3: *Basic Bandgap Reference*

This circuit is also called a "ΔV_{BE}" reference because the differing current densities between matched transistors Q1-Q2 produces a ΔV_{BE} across R3. It works by summing the V_{BE} of Q3 with the amplified ΔV_{BE} of Q1-Q2, developed across R2. The ΔV_{BE} and V_{BE} components have opposite polarity TCs; ΔV_{BE} is proportional-to-absolute-temperature (PTAT), while V_{BE} is complementary-to-absolute-temperature (CTAT). The summed output is V_R, and when it is equal to 1.205 V (silicon bandgap voltage), the TC is a minimum.

The bandgap reference technique is attractive in IC designs because of several reasons; among these are the relative simplicity, and the avoidance of Zeners and their noise. However, very important in these days of ever decreasing system power supplies is the fundamental fact that bandgap devices operate at low voltages, i.e., <5 V. Not only are they used for stand-alone IC references, but they are also used within the designs of many other ICs, such as ADCs and DACs.

Buffered forms of 1.2-V two terminal shunt bandgap references, such as the AD589 IC, remain stable under varying load currents. The AD589 (introduced in 1980), a 1.235-V reference, handles 50 μA to 5 mA with an output impedance of 0.6 Ω, and TCs ranging between 10 and 100 ppm/°C. The more recent and functionally similar AD1580, a 1.225-V shunt reference, is in the tiny SOT-23 package and handles the same nominal currents as the AD589, with TCs of 50 and 100 ppm/°C. The ADR510 shunt reference supplies 1.000 V, and the ADR512 supplies 1.200 V.

However, the basic designs of Figure 7.3 suffer from load and current drive sensitivity, plus the fact that the output needs accurate scaling to more useful levels, i.e., 2.5 V, 5 V, etc. The load drive issue is best addressed with the use of a buffer amplifier, which also provides convenient voltage scaling to standard levels.

An improved three-terminal bandgap reference, the AD580 (introduced in 1974) is shown in Figure 7.4. Popularly called the "Brokaw Cell" (see References 2 and 3), this circuit provides on-chip output buffering, which allows good drive capability and standard output voltage scaling. The AD580 was the first precision bandgap based IC reference, and variants of the topology have influenced further generations of both industry standard references such as the REF01, REF02, and REF03 series, as well as more recent ADI bandgap parts such as the REF19x series, the AD680, AD780, the AD1582-85 series, the ADR38x series, the ADR39x series, and recent SC-70 and SOT-23 offerings of improved versions of the REF01, REF02, and REF03 (designated ADR01, ADR02, and ADR03).

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), by virtue of equal load resistors and a closed loop around the buffer op amp. Due to the resultant smaller V_{BE} of the 8× area Q2, R2 in series with Q2 drops the ΔV_{BE} voltage, while R1 (due to the current relationships) drops a PTAT voltage V1:

$$V_1 = 2 \times \frac{R1}{R2} \times \Delta V_{BE} \quad . \qquad \text{Eq. 7.1}$$

The bandgap cell reference voltage V_Z appears at the base of Q1, and is the sum of V_{BE} (Q1) and V_1, or 1.205 V, the bandgap voltage:

$$V_Z = V_{BE(Q1)} + V_1 \qquad \text{Eq. 7.2}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \Delta V_{BE} \qquad \text{Eq. 7.3}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln \frac{J1}{J2} \qquad \text{Eq. 7.4}$$

$$= V_{BE(Q1)} + 2 \times \frac{R1}{R2} \times \frac{kT}{q} \times \ln 8 \qquad \text{Eq. 7.5}$$

$$= 1.205 V \, . \qquad \text{Eq. 7.6}$$

Note that J1 = current density in Q1, J2 = current density in Q2, and J1/J2 = 8.

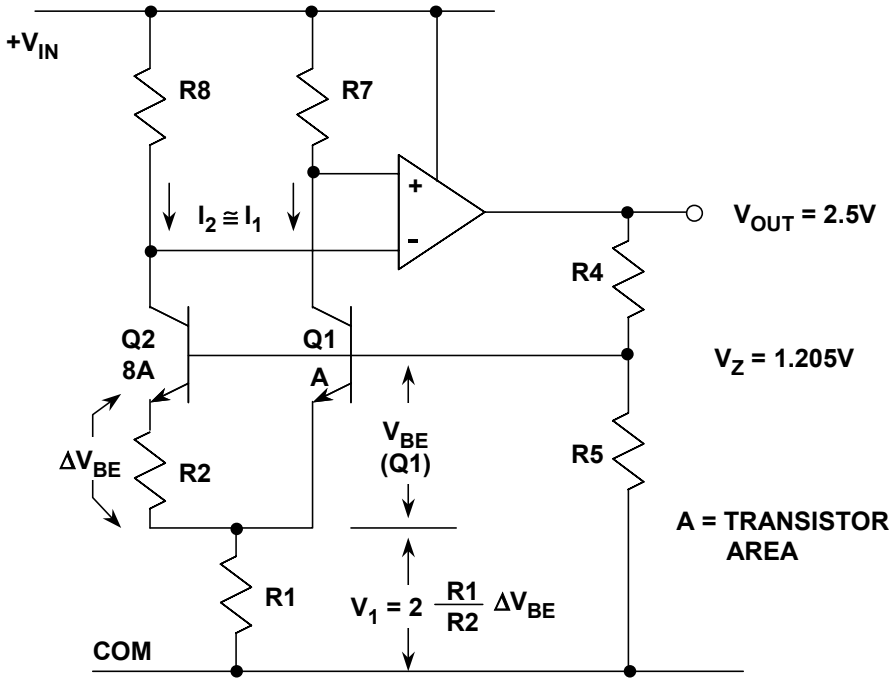


Figure 7.4: *AD580 Precision Bandgap Reference Uses Brokaw Cell (1974)*

However, because of the presence of the R4/R5 (laser trimmed) thin film divider and the op amp, the actual voltage appearing at V_{OUT} can be scaled higher, in the AD580 case 2.5 V. Following this general principle, V_{OUT} can be raised to other practical levels, such as for example in the AD584, with taps for precise 2.5-, 5-, 7.5-, and 10-V operation. The AD580 provides up to 10-mA output current while operating from supplies between 4.5 and 30 V. It is available in tolerances as low as 0.4%, with TCs as low as 10 ppm/°C.

Many of the recent developments in bandgap references have focused on smaller package size and cost reduction, to address system needs for smaller, more power efficient and less costly reference ICs. Among these are several recent bandgap-based IC references.

The AD1580 (introduced in 1996) is a shunt mode IC reference which is functionally quite similar to the classic shunt IC reference, the AD589 (introduced in 1980) mentioned above. A key difference is the fact that the AD1580 uses a newer, small geometry process, enabling its availability within the tiny SOT-23 package. The very small size of this package allows use in a wide variety of space limited applications, and the low operating current lends itself to portable battery powered uses. The AD1580 circuit is shown in simplified form in Figure 7.5.

In this circuit, transistors Q1 and Q2 form the bandgap core, and are operated at a current ratio of 5 times, determined by the ratio of R7 to R2. An op amp is formed by the differential pair Q3-Q4, current mirror Q5, and driver/output stage Q8-Q9. In closed loop equilibrium, this amplifier maintains the bottom ends of R2-R7 at the same potential.

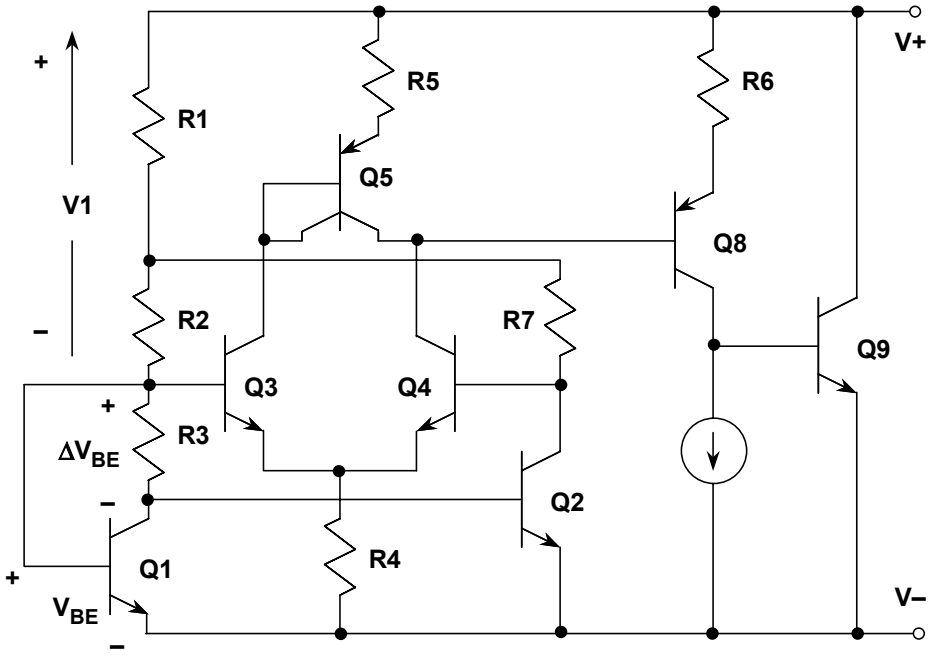


Figure 7.5: *AD1580 1.2-V Shunt Type Bandgap Reference has Tiny Size in SOT-23 Footprint*

As a result of the closed loop control described, a basic ΔV_{BE} voltage is dropped across R3, and a scaled PTAT voltage also appears as V1, which is effectively in series with V_{BE}. The nominal bandgap reference voltage of 1.225 V is then the sum of Q1's V_{BE} and V1. The AD1580 is designed to operate at currents as low as 50 µA, also handling maximum currents as high as 10 mA. It is available in grades with voltage tolerances of ±1 or ±10 mV, and with corresponding TCs of 50 or 100 ppm/°C. Newer members of the Analog Devices' family of shunt regulators are the ADR510 (1.000 V), and the ADR512 (1.200 V).

The ADR520 (2.048 V), ADR525 (2.500 V), ADR530 (3.000 V), ADR540 (4.096 V), ADR545 (4.5 V), and ADR550 (5.0 V) are the latest in the shunt regulator family, with initial accuracies of 0.2%, and available in either SC-70 or SOT-23 packages.

The AD1582-AD1585 series comprises a family of *series* mode IC references, which produce voltage outputs of 2.5, 3.0, 4.096 and 5.0 V. Like the AD1580, the series uses a small geometry process to allow packaging within an SOT-23. The AD1582 series specifications are summarized in Figure 7.6.

The circuit diagram for the series, shown in Figure 7.7, may be recognized as a variant of the basic Brokaw bandgap cell, as described under Figure 7.4. In this case Q1-Q2 form the core, and the overall loop operates to produce the stable reference voltage V_{BG} at the base of Q1. A notable difference here is that the op amp's output stage is designed with push-pull common-emitter stages. This has the effect of requiring an output capacitor for stability, but it also provides the IC with relatively low dropout operation.

The low dropout feature means essentially that V_{IN} can be lowered to as close as several hundred mV above the V_{OUT} level without disturbing operation. The push-pull operation also means that this device series can actually both sink and source currents at the output, as opposed to the classic reference operation of sourcing current (only). For the various output voltage ratings, the divider R5-R6 is adjusted for the respective levels.

- **V_{OUT} : 2.500, 3.000, 4.096, & 5.000V**
- **2.7V to 12V Supply Range (200mV Headroom)**
- **Supply Current : 65µA max**
- **Initial Accuracy: ±0.1% max**
- **Temperature Coefficient: 50 ppm/°C max**
- **Noise: 70µV p-p (0.1Hz - 10Hz)**
- **Noise: 50µV rms (10Hz - 10kHz)**
- **Long-Term Drift: 100ppm/1khrs**
- **High Output Current: ±5mA min**
- **Temperature Range –40°C to +85°C**
- **Low Cost SOT-23 Package**

Figure 7.6: *AD1582-AD1585 2.5-V to 5-V Series-Type Bandgap Reference Specifications*

The AD1582-series is designed to operate with quiescent currents of only 65 µA (maximum), which allows good power efficiency when used in low power systems with varying voltage inputs. The rated output current for the series is 5 mA, and they are available in grades with voltage tolerances of ±0.1 or ±1% of V_{OUT}, with corresponding TCs of 50 or 100 ppm/°C.

Because of stability requirements, devices of the AD1582 series must be used with both an output and input bypass capacitor. Recommended optimum values for these are shown in the hookup diagram of Figure 7.8. For the electrical values noted, it is likely that tantalum chip capacitors will be the smallest in size.

ADR38x and ADR39x-series are low dropout (300 mV) bandgap references in SOT-23 packages. Noise is typically 5-µV p-p in the 0.1 Hz to 10 Hz bandwidth. Quiescent current is typically 100 µA, and the ADR39x-series have a shutdown pin (shutdown current < 3 µA) as well as a "sense" pin for Kelvin sensing. A connection diagram for the ADR39x series is shown in Figure 7.9, and key specifications for the family are shown in Figure 7.10. The ADR38x and ADR39x-series do not require an output capacitor for stability, regardless of the load conditions. However, at least a 1-µF capacitor is recommended to filter out noise. Larger capacitors may be desirable to act as a source of stored energy for transient loads.

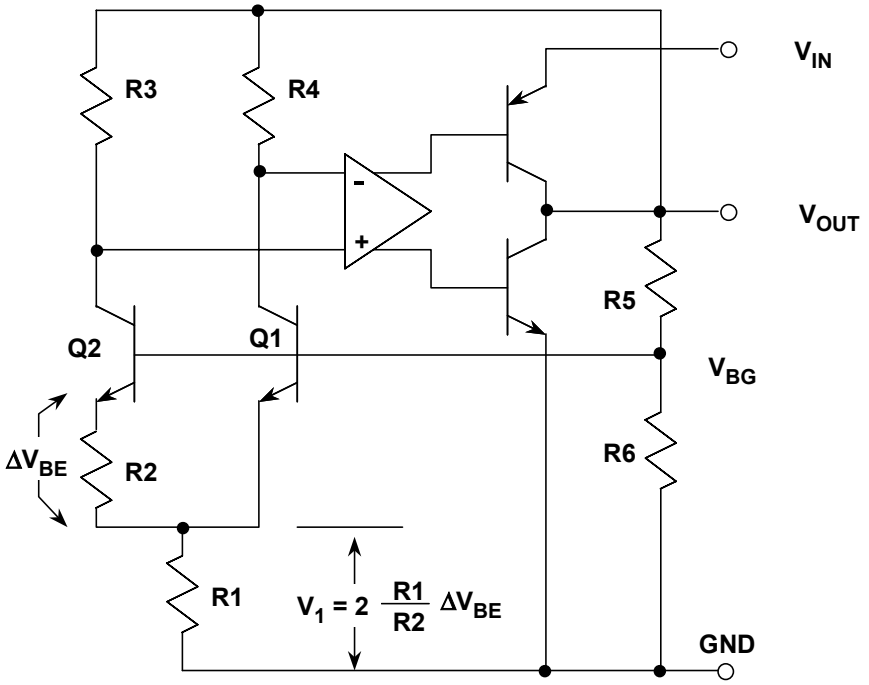
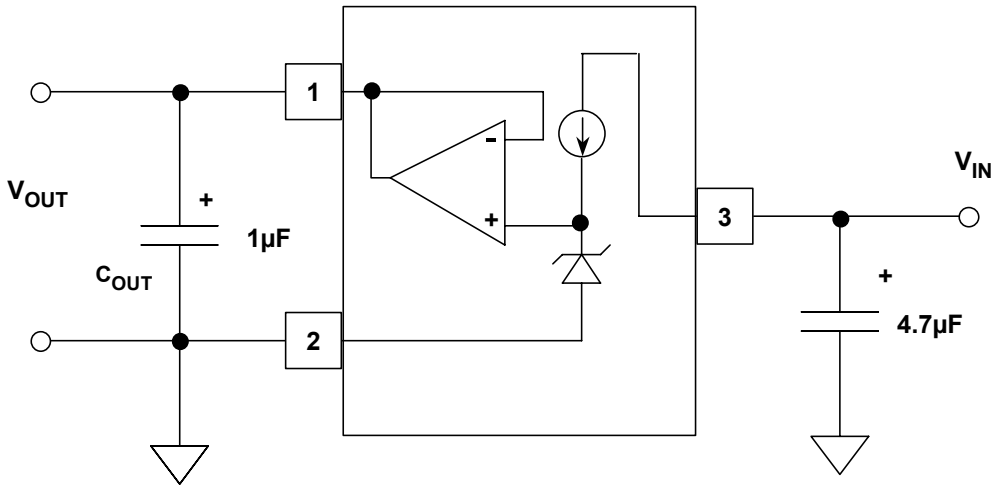


Figure 7.7: *AD1582-AD1585 2.5-V to 5-V Series-Type Bandgap References in SOT-23 Footprint*



AD1582-1585: C_{OUT} REQUIRED FOR STABILITY
ADR380, ADR381: C_{OUT} RECOMMENDED TO ABSORB TRANSIENTS

Figure 7.8: *AD1582-AD1585 Series Connection Diagram*

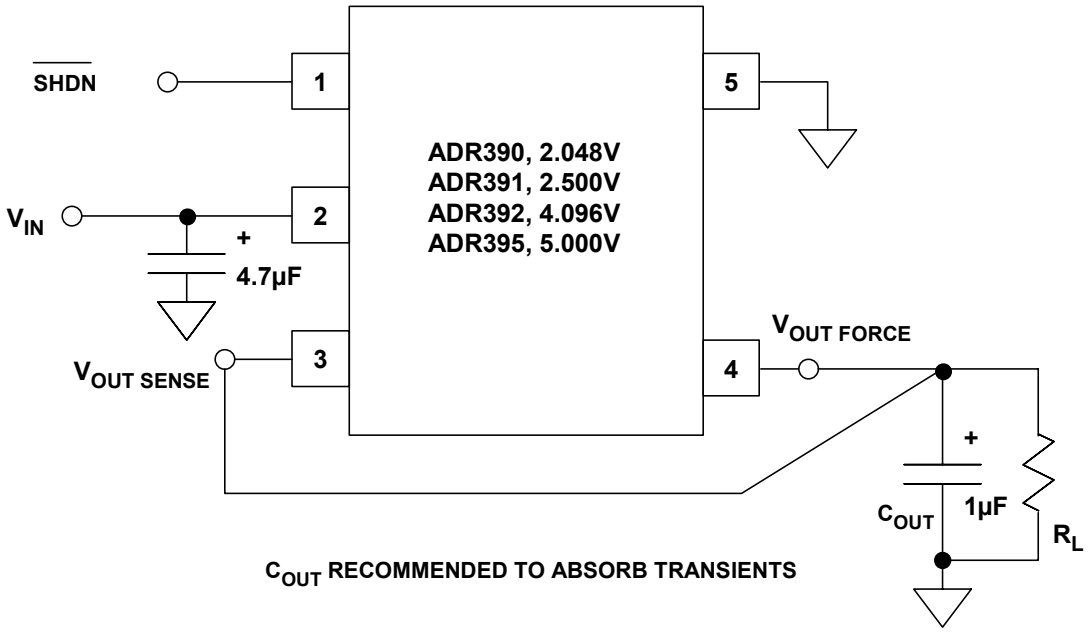


Figure 7.9: *ADR390, ADR391, ADR392, ADR395 Connection Diagram*

- **V_{OUT} : 2.048, 2.500, 4.096, & 5.000V**
- **2.3V to 15V Supply Range (300mV Headroom)**
- **Supply Current : 120µA max**
- **Initial Accuracy: ±6mV max**
- **Temperature Coefficient: 25 ppm/°C max**
- **Noise: 5µV p-p (0.1Hz - 10Hz)**
- **Long-Term Drift: 50ppm/1khrs**
- **High Output Current: +5mA min**
- **Temperature Range –40°C to +85°C**
- **Shutdown Feature: <3µA max**
- **Kelvin Sensing (Force and Sense Pins)**
- **Low Cost SOT-23 (5 pin) Package**

Figure 7.10: *ADR390-ADR395 2.048-V to 5-V Series-Type Bandgap Reference Specifications*

Buried Zener References

In terms of the design approaches used within the reference core, the two most popular basic types of IC references consist of the bandgap and buried Zener units. Bandgaps have been discussed, but Zener based references warrant some further discussion.

In an IC chip, surface operated diode junction breakdown is prone to crystal imperfections and other contamination, thus Zener diodes formed at the surface are more noisy and less stable than are *buried* (or sub-surface) ones. ADI Zener based IC references employ the much preferred buried Zener. This improves substantially upon the noise and drift of surface-mode operated Zeners (see Reference 4). Buried Zener references offer very low temperature drift, down to the 1-2 ppm/°C (AD588 and AD586), and the lowest noise as a percent of full-scale, i.e., 100 nV/√Hz or less. On the downside, the operating current of Zener type references is usually relatively high, typically on the order of several mA.

An important general point arises when comparing noise performance of different references. The best way to do this is to compare the ratio of the noise (within a given bandwidth) to the dc output voltage. For example, a 10-V reference with a 100-nV/√Hz noise density is 6-dB more quiet in relative terms than is a 5-V reference with the same noise level.

XFET® References

A third and relatively new category of IC reference core design is based on the properties of junction field effect (JFET) transistors. Somewhat analogous to the bandgap reference for bipolar transistors, the JFET based reference operates a pair of junction field effect transistors with different pinchoff voltages, and amplifies the differential output to produce a stable reference voltage. One of the two JFETs uses an extra ion implantation, giving rise to the name XFET® (eXtra implantation junction Field Effect Transistor) for the reference core design.

The basic topology for the XFET reference circuit is shown in Figure 7.11. J1 and J2 are the two JFET transistors, which form the core of the reference. J1 and J2 are driven at the same current level from matched current sources, I1 and I2. To the right, J1 is the JFET with the extra implantation, which causes the difference in the J1-J2 pinchoff voltages to differ by 500 mV. With the pinchoff voltage of two such FETs purposely skewed, a differential voltage will appear between the gates for identical current drive conditions and equal source voltages. This voltage, ΔV_P, is:

$$\Delta V_P = V_{P1} - V_{P2} , \qquad \text{Eq. 7.7}$$

where V_{P1} and V_{P2} are the pinchoff voltages of FETs J1 and J2, respectively.

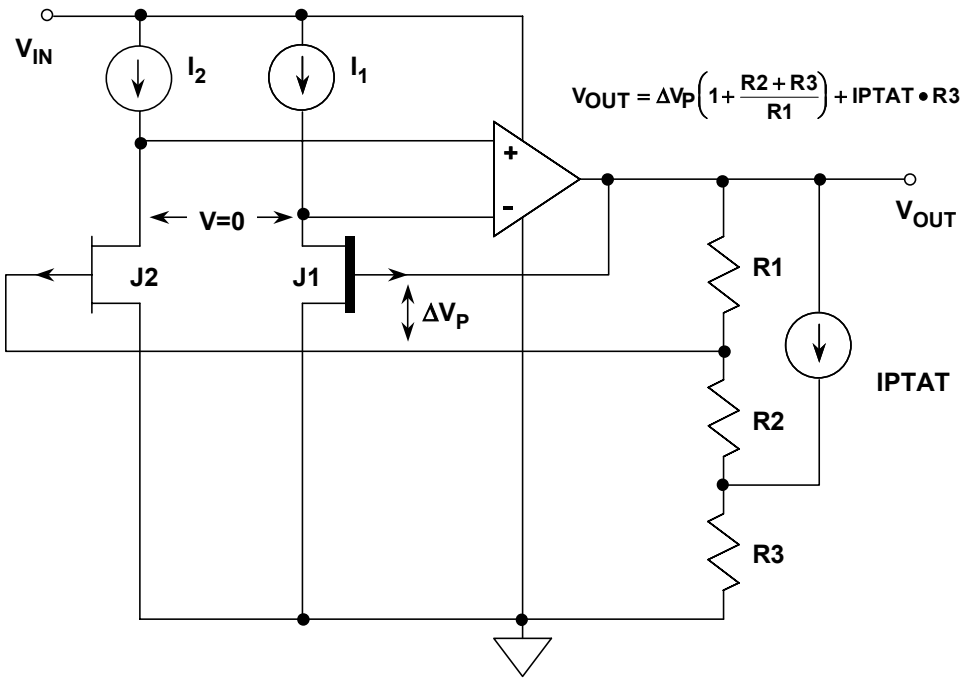


Figure 7.11: *ADR290-ADR293 2.048-V to 5-V XFET® References Feature High Stability and Low Power*

Note that, within this circuit, the voltage ΔV_P exists between the *gates* of the two FETs. We also know that, with the overall feedback loop closed, the op amp axiom of zero input differential voltage will hold the sources of the two JFETs at the same potential. These source voltages are applied as inputs to the op amp, the output of which drives feedback divider R1-R3. As this loop is configured, it stabilizes at an output voltage from the R1-R2 tap which does in fact produce the required ΔV_P between the J1-J2 gates. In essence, the op amp amplifies ΔV_P to produce V_{OUT},where

$$V_{OUT} = \Delta V_P\left(1+\frac{R2+R3}{R1}\right)+(I_{PTAT})(R3). \qquad \text{Eq. 7.8}$$

As can be noted, this expression includes the basic output scaling (leftmost portion of the right terms), plus a rightmost temperature dependent term including I_{PTAT}. The I_{PTAT} portion of the expression compensates for a basic negative temperature coefficient of the XFET core, such that the overall net temperature drift of the reference is typically in a range of 3 to 8 ppm/°C.

During manufacture, the R1-R3 scaling resistance values are adjusted to produce the different voltage output options of 2.048, 2.5, 4.096 and 5.0 V for the ADR290, ADR291, ADR292 and ADR293 family (ADR29x). This ADR29x family of series mode references is available in 8 pin packages with a standard footprint. They operate from supplies of V_{OUT} plus 500 mV to 15 V, with a maximum quiescent current of 12 µA, and output currents of up to 5 mA. A summary of specifications for the family appears in Figure 7.12.

- **V_{OUT} : 2.048, 2.500, 4.096, & 5.000V**
- **2.7V to 15V Supply Range (0.5V Headroom)**
- **Supply Current : 12µA max**
- **Initial Accuracy: ±0.1%**
- **Temperature Coefficient: 8 ppm/°C max**
- **Low-Noise: 6µV p-p (0.1 - 10Hz)**
- **Wideband Noise: 420nV/√Hz @ 1kHz**
- **Long-Term Drift: 50ppm/1000 hours**
- **High Output Current: 5mA min**
- **Temperature Range –40°C to +125°C**
- **Standard REF02 Pinout**
- **8-Lead Narrow Body SOIC, 8-Lead TSSOP**

Figure 7.12: *ADR290-ADR293 XFET® Series Specifications*

The ADR43x-series are the second generation of low noise, low drift XFET references. Standard voltage outputs are 2.048, 2.500, 3.000, 4.096, and 5.000 V. These devices operate from supplies of V_{OUT} + 1 V to 18 V with quiescent currents of 0.5-mA maximum and output currents of ±10 mA. Temperature drift is 3-ppm/°C maximum. The 0.1-Hz to 10-Hz noise is an incredibly low 1.5-µV p-p. This ADR43x family of series mode references is available in 8 pin packages with a standard footprint. Key specifications for the family are summarized in Figure 7.13.

- **V_{OUT} : 2.048, 2.500, 3.000, 4.096, & 5.000V**
- **3V to 18V Supply Range (1V Headroom)**
- **Supply Current : 500µA**
- **Initial Accuracy: ±0.05%**
- **Temperature Coefficient: 3 ppm/°C max**
- **Low-Noise: 1.75µV p-p (0.1 - 10Hz)**
- **Wideband Noise: 60nV/√Hz @ 1kHz**
- **Long-Term Drift: 50ppm/1000 hours**
- **High Output Current: ±10mA min**
- **Temperature Range –40°C to +125°C**
- **8-Lead MSOP, 8-Lead TSSOP**

Figure 7.13: *ADR430-ADR439 XFET® Series Specifications*

The XFET architecture offers performance improvements over bandgap and buried Zener references, particularly for systems where operating current is critical, yet drift and noise performance must still be excellent. XFET noise levels are lower than bandgap based bipolar references operating at an equivalent current, the temperature drift is low and linear at 3-8 ppm/°C (allowing easier compensation when required), and the series has lower hysteresis than bandgaps. Thermal hysteresis is a low 50 ppm over a –40°C to +125°C range, less that half that of a typical bandgap device. Finally, the long-term stability is excellent, typically only 50 ppm/1000 hours.

Figure 7.14 summarizes the pro and con characteristics of the three reference architectures; bandgap, buried Zener, and XFET.

BANDGAP	BURIED ZENER	XFET®
< 5V Supplies	> 5V Supplies	< 5V Supplies
High Noise @ High Power	Low Noise @ High Power	Low Noise @ Low Power
Fair Drift and Long Term Stability	Good Drift and Long Term Stability	Excellent Drift and Long Term Stability
Fair Hysteresis	Fair Hysteresis	Low Hysteresis

Figure 7.14: *Characteristics of Reference Architectures*

Modern IC references come in a variety of styles, but series operating, fixed output positive types do tend to dominate. These devices can use bandgap-based bipolars, JFETs, or buried Zeners at the device core, all of which has an impact on the part's ultimate performance and application suitability. They may or may not also be low power, low noise, and/or low dropout, and be available within a certain package. Of course, in a given application, any single one of these differentiating factors can drive a choice, thus it behooves the designer to be aware of all the different devices available.

Figure 7.15 shows the standard footprint for such a series type IC positive reference in an 8 pin package (Note that pin numbers shown refer to the standard pin for that function). There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin (5). Some bandgap references also have a high impedance PTAT output (V_{TEMP}) for temperature sensing (pin 3). The intent here is that no appreciable current be drawn from this pin, but it can be useful for such non-loading types of connections as comparator inputs, to sense temperature thresholds, etc.

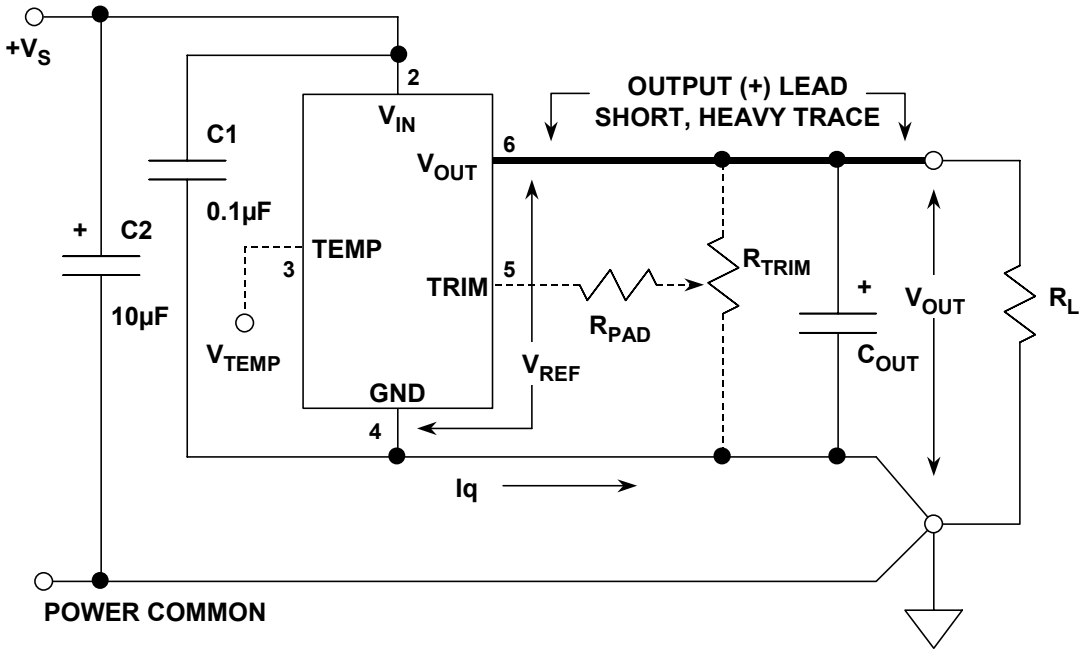


Figure 7.15: *Standard Positive Output Three Terminal Reference Hookup (8-pin DIP Pinout)*

All references should use decoupling capacitors on the input pin (2), but the amount of decoupling (if any) placed on the output (pin 6) depends upon the stability of the reference's output op amp with capacitive load. Simply put, there is no hard and fast rule for capacitive loads here. For example, some three terminal types *require* the output capacitor for stability (i.e., REF19x and AD1582-85 series), while with others it is optional for performance improvement (AD780, REF43, ADR29x, ADR43x, AD38x, AD39x, ADR01, ADR02, ADR03). Even if the output capacitor is optional, it may still be required to supply the energy for transient load currents, as presented by some ADC reference input circuits. The safest rule then is that you should use the data sheet to verify what are the specific capacitive loading ground rules for the reference you intend to use, for the load conditions your circuit presents.

Voltage Reference Specifications

Tolerance

It is usually better to select a reference with the required value and accuracy and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as approximately 0.04% can be achieved with the AD586, AD780, REF195, and ADR43x-series, while the AD588 is 0.01%. If and when trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. When/if additional external scaling is required, a precision op amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

Drift

The XFET and buried Zener reference families have the best long term drift and TC performance. The XFET ADR43x-series have TCs as low as 3 ppm/°C. TCs as low as 1-2 ppm/°C are available with the AD586 and AD588 buried Zener references, and the AD780 bandgap reference is almost as good at 3 ppm/°C.

The XFET series achieve long terms drifts of 50 ppm/1000 hours, while the buried Zener types come in at 25 ppm/1000 hours. Note that where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000-hour figure by 8.77 to find the annual drift—this is not correct, and can in fact be quite pessimistic. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about $\sqrt{8.766} \approx 3$ times the 1000-hour figure, and the ten year value will be roughly 9 times the 1000-hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects fullscale accuracy as shown in Figure 7.16. This table shows system resolution and the TC required to maintain ½ LSB error over an operating temperature range of 100°C. For example, a TC of about 1 ppm/°C is required to maintain ½ LSB error at 12 bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of ½ LSB for popular full scale ranges.

		½ LSB WEIGHT (mV) 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	REQUIRED DRIFT (ppm/°C)	10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 7.16: *Reference Temperature Drift Requirements for Various System Accuracies (1/2 LSB Criteria, 100°C Span)*

Supply Range

IC reference supply voltages range from about 3 V (or less) above rated output, to as high as 30 V (or more) above rated output. Exceptions are devices designed for low dropout, such as the REF19x, AD1582-AD1585, ADR38x, ADR39x series. At low currents, the REF195 can deliver 5 V with an input as low as 5.1 V (100-mV dropout). Note that due to process limits, some references may have more restrictive maximum voltage input ranges, such as the AD1582-AD1585 series (12 V), the ADR29x series (15 V), and the ADR43x series (18 V).

Load Sensitivity

Load sensitivity (or output impedance) is usually specified in μV/mA of load current, or mΩ, or ppm/mA. While figures of 70 ppm/mA or less are quite good (AD780, REF43, REF195, ADR29x, ADR43x), it should be noted that external wiring drops can produce comparable or worse errors at high currents, without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return. For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588, AD688, ADR39x) are used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore the source impedance is a function of frequency. Typical reference output impedance rises at 6 dB/octave from the dc value, and is nominally about 10 Ω at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op amp within the reference remains stable for such loading.

Line Sensitivity

Line sensitivity (or regulation) is usually specified in μV/V, (or ppm/V) of input change, and is typically 25 ppm/V (–92 dB) in the REF43, REF195, AD680, AD780, ADR29x, ADR39x, and ADR43x. For dc and very low frequencies, such errors are easily masked by noise.

As with op amps, the line sensitivity (or power supply rejection) of references degrades with increasing frequency, typically 30 to 50 dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a low dropout pre-regulator, such as one of the ADP3300-series parts.

Figure 7.17 summarizes the major reference specifications along with typical values available.

- **Tolerance:**
  - **AD588** — **0.01%**
  - **ADR43x, AD780, REF195** — **0.04%**
- **Drift (TC):**
  - **AD586, AD588** — **1-2ppm/°C**
  - **AD780, ADR42x, ADR43x, ADR01, ADR02, ADR03** — **3 ppm/°C**
- **Drift (long term):**
  - **ADR29x,ADR42x, ADR43x** — **50 ppm/1000 hours**
  - **AD588** — **25 ppm/1000 hours**
- **Supply Range:**
  - **REF19x, ADR38x, ADR39x, AD158x, AD780** — **V_{OUT} plus 0.3V-15V**
- **Load Sensitivity** — **70ppm/mA (350mΩ @ 5V)**
- **Line Sensitivity** — **25ppm/V (–92 dB @ 5V)**

Figure 7.17: *Voltage Reference DC Specifications (Typical Values Available)*

Noise

Reference noise is not always specified, and when it is, there is not total uniformity on how it is measured. For example, some devices are characterized for peak-to-peak noise in a 0.1-Hz to 10-Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op amps) is a plot of noise voltage spectral density (nV/√Hz) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of 6.6 × rms is used to define a practical peak value—statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than ½ LSB in order to maintain required accuracy. If peak-to-peak noise is assumed to be 6 times the rms value, then for an N-bit system, reference voltage fullscale V_{REF}, reference noise bandwidth (BW), the required noise voltage spectral density E_n (V/√Hz) is given by:

$$E_n \leq \frac{V_{REF}}{12 \cdot 2^N \cdot \sqrt{BW}}. \qquad \text{Eq. 7.9}$$

For a 10-V, 12-bit, 100-kHz system, the noise requirement is a modest 643 nV/√Hz. Figure 7.18 shows that increasing resolution and/or lower fullscale references make noise

requirements more stringent. The 100-kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC references have noise spectral densities around 100 nV/√Hz, so additional filtering is obviously required in most high resolution systems, especially those with low values of V_{REF}.

	NOISE DENSITY (nV/√Hz) FOR 10, 5, AND 2.5V FULLSCALE RANGES		
BITS	**10V**	**5V**	**2.5V**
12	**643**	**322**	**161**
13	**322**	**161**	**80**
14	**161**	**80**	**40**
15	**80**	**40**	**20**
16	**40**	**20**	**10**

Figure 7.18: *Reference Noise Requirements for Various System Accuracies (1/2-LSB / 100-kHz Criteria)*

Some references, for example the AD587 buried Zener type have a pin designated as the *noise reduction pin* (see data sheet). This pin is connected to a high impedance node preceding the on-chip buffer amplifier. Thus an externally connected capacitor C_N will form a low pass filter with an internal resistor, to limit the effective noise bandwidth seen at the output. A 1-µF capacitor gives a 3-dB bandwidth of 40 Hz. Note that this method of noise reduction is by no means universal, and other devices may implement noise reduction differently, if at all.

There are also general purpose methods of noise reduction, which can be used to reduce the noise of any reference IC, at any standard voltage level. The reference circuit of Figure 7.19 (References 5 and 6) is one such example. This circuit uses external filtering and a precision low-noise op amp to provide both very low noise and high dc accuracy. Reference U1 is a 2.5-, 3.0-, 5-, or 10-V reference with a low noise buffered output. The output of U1 is applied to the R1-C1/C2 noise filter to produce a corner frequency of about 1.7 Hz. Electrolytic capacitors usually imply dc leakage errors, but the bootstrap connection of C1 causes its applied bias voltage to be only the relatively small drop across R2. This lowers the leakage current through R1 to acceptable levels. Since the filter attenuation is modest below a few Hertz, the reference noise still affects overall performance at low frequencies (i.e., <10 Hz).

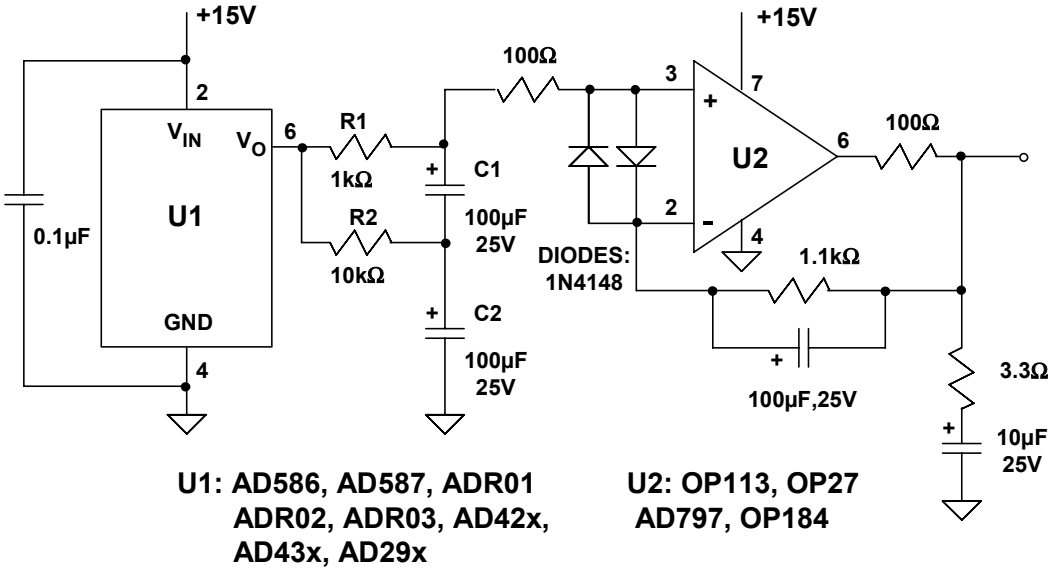


Figure 7.19: *Combining Low-noise Amplifier with Extensive Filtering Yields Exceptional Reference Noise Performance of (1.5 to 5 nV) /√Hz @ 1 kHz*

The output of the filter is then buffered by a precision low noise unity-gain follower, such as the OP113EP. With less than ±150-µV offset error and under 1-µV/°C drift, the buffer amplifier's dc performance will not seriously affect the accuracy/drift of most references. For example, an ADR292E for U1 will have a typical drift of 3 ppm/°C, equivalent to 7.5 µV/°C, higher than the buffer amplifier.

Almost any op amp will have a current limit higher than a typical IC reference. Further, even lower noise op amps are available for 5- to 10-V use. The AD797 offers 1-kHz noise performance less than 2 nV/√Hz in this circuit, compared to about 5 nV/√Hz for the OP113. With any amplifier, Kelvin sensing can be used at the load point, a technique which can eliminate I×R related output voltage errors.

Scaled References

A useful approach when a non-standard reference voltage is required is to simply buffer and scale a basic low voltage reference diode. With this approach, a potential difficulty is getting an amplifier to work well at such low voltages as 3 V. A workhorse solution is the low power reference and scaling buffer shown in Figure 7.20. Here a low current 1.2-V two terminal reference diode is used for D1, which can be either a 1.200-V ADR512, 1.235-V AD589, or the 1.225-V AD1580. Resistor R1 sets the diode current in either case, and is chosen for the diode minimum current requirement at a minimum supply of 2.7 V. Obviously, loading on the unbuffered diode must be minimized at the V_{REF} node.

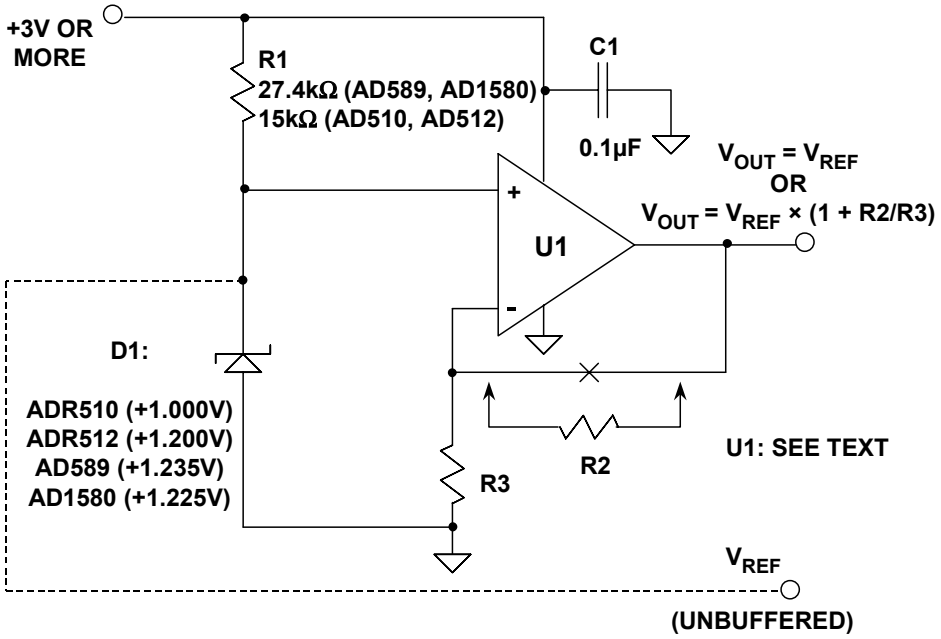


Figure 7.20: *Rail-to-rail Output Op Amps Allow Greatest Flexibility in Low Dropout References*

The amplifier U1 both buffers and optionally scales up the nominal 1.0 or 1.2-V reference, allowing much higher source/sink output currents. Of course, a higher op amp quiescent current is expended in doing this, but this is a basic tradeoff of the approach. Quiescent current is amplifier dependent, ranging from 45 µA/channel with the OP196/296/496 series to 1000-2000 µA/channel with the OP284 and OP279. The former series is most useful for very light loads (<2 mA), while the latter series provide device dependent outputs up to 50 mA. Various devices can be used in the circuit as shown, and their key specs are summarized in Figure 7.21.

DEVICE*	Iq, mA per channel	Vsat (+) V (min @ mA)	Vsat (–) V (max @ mA)	Isc, mA min
OP281/481	0.003	4.93 @ 0.05	0.075 @ 0.05	± 3.5
OP193/293	0.017	4.20 @ 1	0.280 @ 1 (typ)	± 8
OP196/296/496	0.045	4.30 @ 1	0.400 @ 1	± 4 (typ)
AD8541/42/44	0.045	4.97 @ 1	0.025 @ 1	± 60
OP777	0.220	4.91 @ 1	0.126 @ 1	± 10
AD820/822	0.620	4.89 @ 2	0.055 @ 2	± 15
OP184/284/484	1.250**	4.85 @ 2.5	0.125 @ 2.5	± 7.5
AD8531/32/34	1.400	4.90 @ 10	0.100 @ 10	± 250

*** Typical device specifications @ Vs = +5V, TA = 25°C, unless otherwise noted**
**** Maximum**

Figure 7.21: *Op Amps Useful in Low Voltage Rail-Rail References and Regulators*

In Figure 7.20, without gain scaling resistors R2-R3, V_{OUT} is simply equal to V_{REF}. With the use of the scaling resistors, V_{OUT} can be set anywhere between a lower limit of V_{REF}, and an upper limit of the positive rail, due to the op amp's rail-rail output swing. Also, note that this buffered reference is inherently low dropout, allowing a +4.5-V (or more) reference output on a +5-V supply, for example. The general expression for V_{OUT} is shown in the figure, where V_{REF} is the reference voltage.

Amplifier standby current can be further reduced below 20 μA, if an amplifier from the OP181/281/481 or the OP193/293/493 series is used. This choice will be at some expense of current drive, but can provide very low quiescent current if necessary. All devices shown operate from voltages down to 3 V (except the OP279, which operates at 5 V).

Voltage Reference Pulse Current Response

The response of references to dynamic loads is often a concern, especially in applications such as driving some ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-delta ADC may be the switched capacitor circuit shown in Figure 7.22. The dynamic load causes current spikes in the reference as the capacitor C_{IN} is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

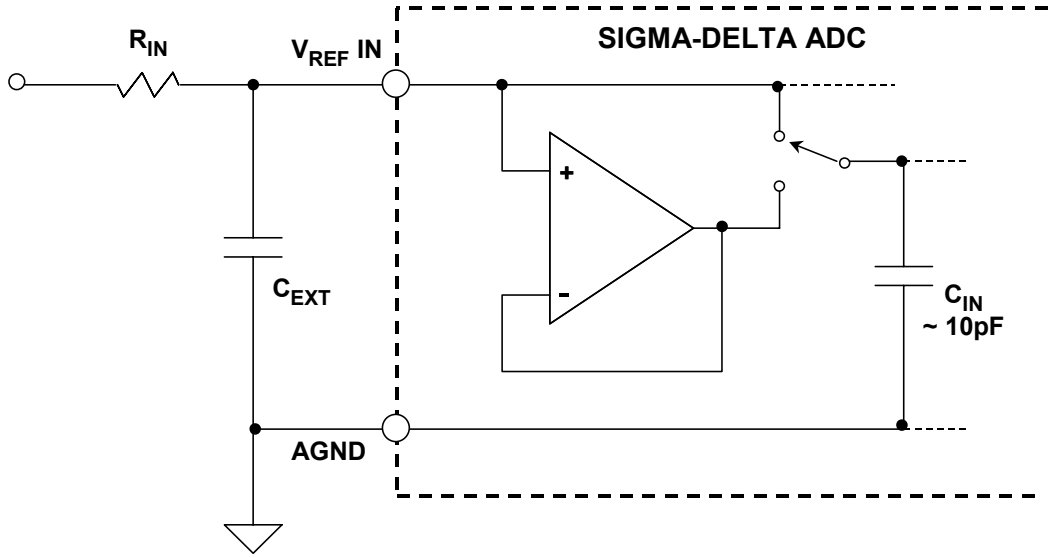


Figure 7.22: *Switched Capacitor Input of Sigma-Delta ADC Presents a Dynamic Load to the Voltage Reference*

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. Thus it is important to maintain a low noise, transient free potential at the ADC's reference input. Be aware that if the reference source impedance is too high, dynamic loading can cause the reference input to shift by more than 5 mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads. Therefore it is quite

important to verify that the device chosen will satisfactorily drive the output capacitance required. In any case, the converter reference inputs should always be decoupled—with at least 0.1 µF, and with an additional 5-50 µF if there is any low frequency ripple on its supply. See Figure 7.15 (again).

Since some references misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 7.23. In a typical voltage reference, a step change of 1 mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a 0.01-µF capacitor is connected to the reference output.

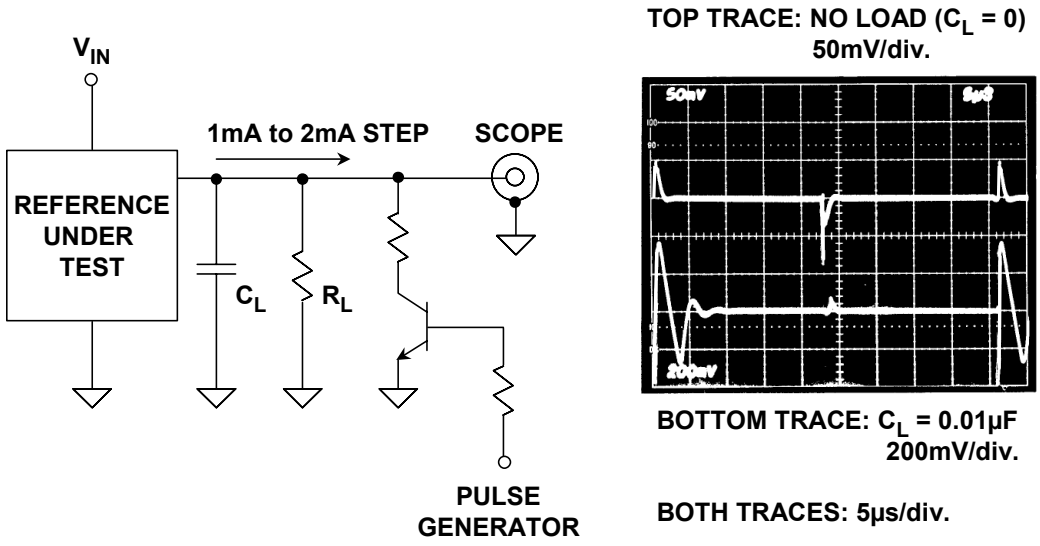


Figure 7.23: *Make Sure Reference is Stable with Large Capacitive Loads*

Where possible, a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation, it has excellent drift and an accurate output, in addition to relatively low power consumption. Other references which are useful with output capacitors are the REF19x, the AD1582-AD1585 series, the ADR29x-series, and the ADR43x-series.

As noted above, reference bypass capacitors are useful when driving the reference inputs of successive-approximation ADCs. Figure 7.24 illustrates reference voltage settling behavior immediately following the "Start Convert" command. A small capacitor (0.01 µF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. As shown by the bottom trace, decoupling with a ≥ 1-µF capacitor maintains the reference stability during conversion.

Where voltage references are required to drive large capacitances, it is also critically important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the reference output reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the same reference in a low capacitance loaded state.

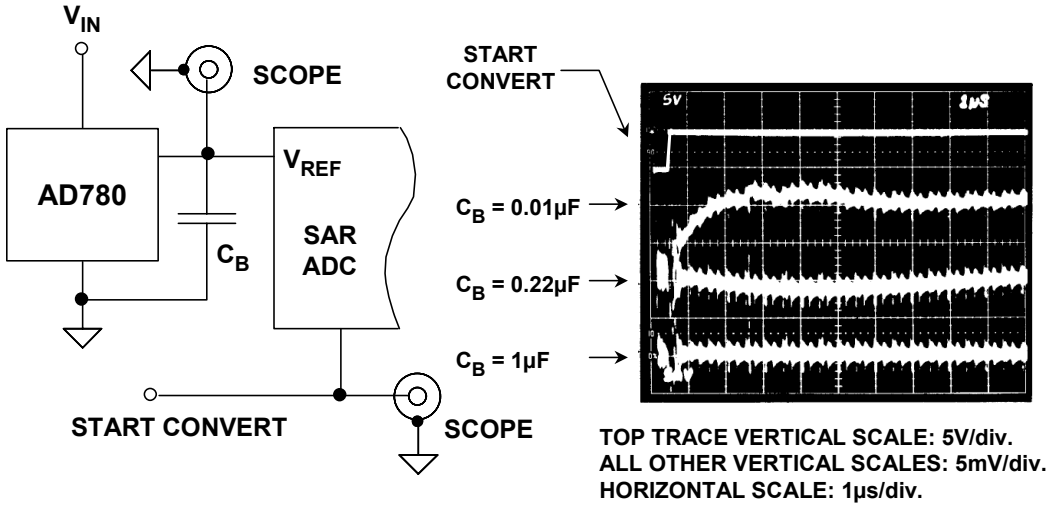


Figure 7.24: *Successive Approximation ADCs Can Present a Dynamic Transient Load to the Reference*

Low Noise References for High Resolution Converters

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. In such cases, using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5-V internal reference with a 0.1-Hz to 10-Hz noise of 8.3-µV rms (2600 nV/√Hz), while the AD780 reference noise is only 0.67 µV rms (200 nV/√Hz). The internal noise of the AD7710-series in this bandwidth is about 1.7-µV rms. The use of the AD780 increases the effective resolution of the AD7710 from about 20.5 bits to 21.5 bits.

Figure 7.25 shows the low noise ADR431 used as the +2.5-V reference for the AD77xx-series ADCs. Optimally, the use of the ADR433 (3-V output) enhances the dynamic range of the ADC, while lowering overall system noise as described above. In addition, the ADR43x-series allow a large decoupling capacitor on its output thereby minimizing conversion errors due to transients.

There is one possible but yet quite real problem when replacing the internal reference of a converter with a higher precision external one. The converter in question may have been trimmed during manufacture to deliver its specified performance with a relatively inaccurate internal reference. In such a case, using a more accurate external reference with the converter may actually introduce additional gain error! For example, the early AD574 had a guaranteed uncalibrated gain accuracy of 0.125% when using an internal 10-V reference (which itself had a specified accuracy of only ±1%). It is obvious that if such a device, having an internal reference which is at one end of the specified range, is used with an external reference of exactly 10 V, then its gain will be about 1% in error.

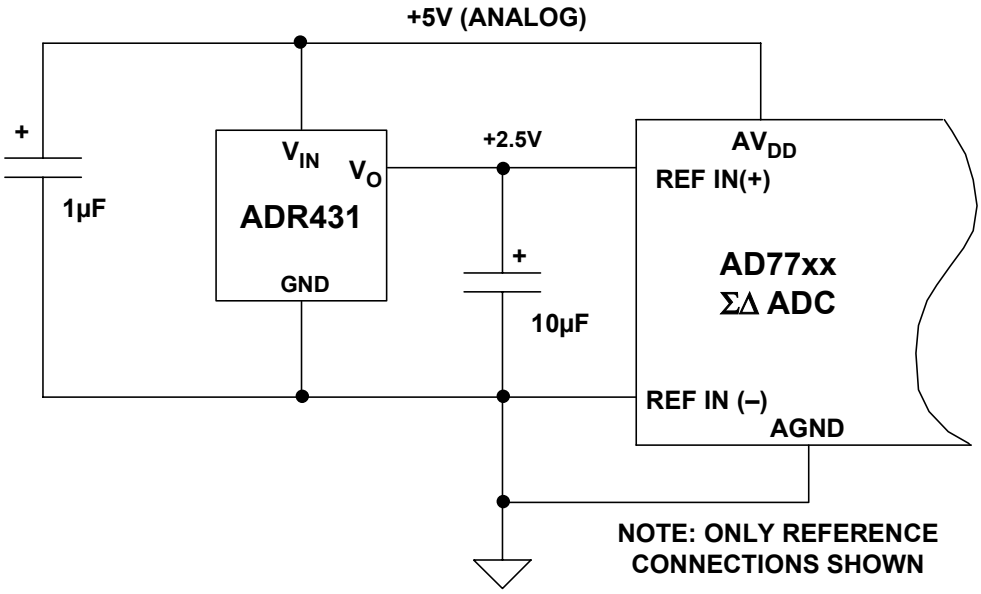


Figure 7.25: *The AD431 XFET Reference is Ideal for Driving Precision Sigma-Delta ADCs*

REFERENCES:
7.1 VOLTAGE REFERENCES

1. Bob Widlar, "New Developments in IC Voltage Regulators," **IEEE Journal of Solid State Circuits**, Vol. SC-6, February, 1971.

2. Paul Brokaw, "A Simple Three-Terminal IC Bandgap Voltage Reference," **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

3. Paul Brokaw, "More About the AD580 Monolithic IC Voltage Regulator," **Analog Dialogue**, 9-1, 1975.

4. Dan Sheingold, Section 20.2 within **Analog-Digital Conversion Handbook, 3d. Edition**, Prentice-Hall, 1986.

5. Walt Jung, "Build an Ultra-Low-Noise Voltage Reference," **Electronic Design Analog Applications Issue**, June 24, 1993.

6. Walt Jung, "Getting the Most from IC Voltage References," **Analog Dialogue**, 28-1, 1994, pp. 13-21.

SECTION 7.2: LOW DROPOUT LINEAR REGULATORS

Walt Jung

Introduction

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5-V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 1.5 to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. One reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2 V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the *low drop out* regulator, or more popularly, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0-V LDO output drops to 4.9 V (–2%) under conditions of an input-output differential of 0.5 V, by this definition the LDO's V_{MIN} is 0.5 V.

As will be shown in this section, dropout voltage is extremely critical to a linear regulator stage's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes this lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems that must provide stable voltages from batteries, such as portable computers, cellular phones, etc. This is simply because they maintain their regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw dc supplies, LDOs allow lower transformer secondary voltages, reducing system susceptibility to shutdown under brownout conditions as well as allowing cooler operation.

Linear Voltage Regulator Basics

A brief review of three terminal linear IC regulator fundamentals is necessary to understanding the LDO variety. As it turns out, almost all LDOs available today, as well as many of the more general three terminal regulator types, are *positive leg, series style* regulators. This simply means that they control the regulated voltage output by means of a pass element which is in series with the positive side of the unregulated input.

This is shown more clearly in Figure 7.26, which is a hookup diagram for a hypothetical three terminal style regulator. To reiterate what was said earlier in the chapter about reference ICs, in terms of their basic functionality, many standard voltage regulator ICs are available in the series three-terminal form as is shown here (V_{IN}, GND or Common, V_{OUT}).

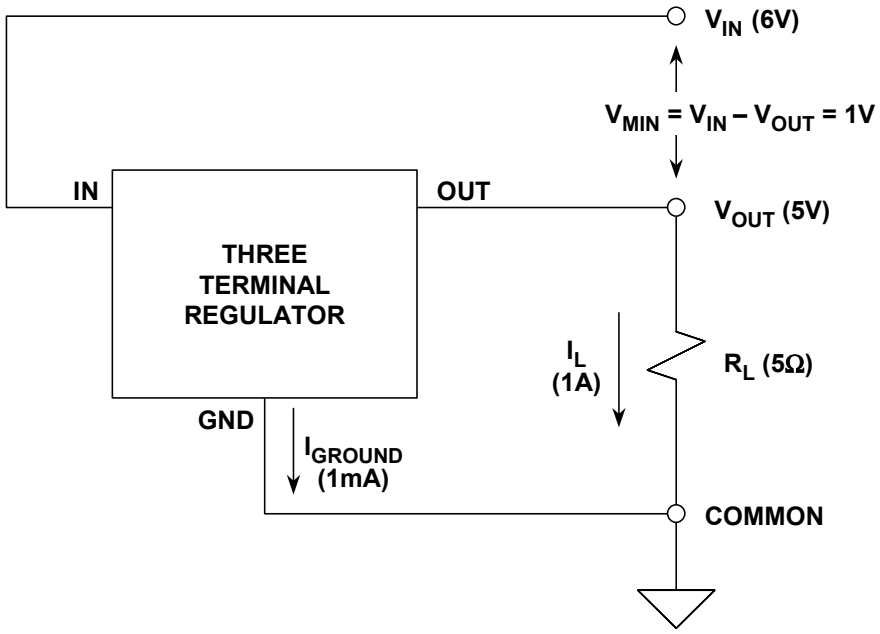


Figure 7.26: *A Basic Three Terminal Voltage Regulator*

This diagram also allows some statements to be made about power losses in the regulator. There are two components to power which are dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and I_{ground}. If we call the total power P_D, this then becomes:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(I_{ground}). \qquad \text{Eq. 7.10}$$

Obviously, the magnitude of the load current and the regulator dropout voltage both greatly influence the power dissipated. However, it is also easy to see that for a given I_L, as the dropout voltage is lowered, the first term of P_D is reduced. With an intermediate dropout voltage rating of 1 V, a 1-A load current will produce 1 W of heat in this regulator, which will require a heat sink for continuous operation. It is this first term of the regulator power which usually predominates, at least for loaded regulator conditions.

The second term, being proportional to I_{ground} (typically only 1-2 mA, sometimes even less) usually only becomes significant when the regulator is unloaded, and the regulator's quiescent or standby power then produces a constant drain on the source V_{IN}.

However, it should be noted that in some types of regulators (notably those which have very low β pass devices such as lateral PNP transistors) the I_{ground} current under load can actually run quite high. This effect is worst at the onset of regulation, or when the pass device is in saturation, and can be noted by a sudden I_{ground} current "spike", where the current jumps upward abruptly from a low level. All LDO regulators using bipolar transistor pass devices which can be saturated (such as PNPs) can show this effect. It is much less severe in PNP regulators using vertical PNPs (since these have a higher intrinsic β) and doesn't exist to any major extent in PMOS LDOs (since PMOS transistors are controlled by voltage level, not current).

In the example shown, the regulator delivers 5 V × 1 A, or 5 W to the load. With a dropout voltage of 1 V, the input power is 6-V times the same 1 A, or 6 W. In terms of power efficiency, this can be calculated as:

$$P_{EFF}(\%) = 100 \times \frac{P_{OUT}}{P_{IN}}, \qquad \text{Eq. 7.11}$$

where P_{OUT} and P_{IN} are the total output and input powers, respectively.

In these sample calculations, the relatively small portion of power related to I_{ground} will be ignored for simplicity, since this power is relatively small. In an actual design, this simplifying step may not be justified.

In the case shown, the efficiency would be 100 × 5/6, or about 83%. But by contrast, if an LDO were to be used with a dropout voltage of 0.1 V instead of 1 V, the input voltage can then be allowed to go as low as 5.1 V. The new efficiency for this condition then becomes 100 × 5/5.1, or 98%. It is obvious that an LDO can potentially greatly enhance the power efficiency of linear voltage regulator systems.

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 7.27.

In this diagram virtually all of the elements shown can be considered to be fundamentally necessary, the exceptions being the shutdown control and saturation sensor functions (shown dotted). While these are present on many current regulators, the shutdown feature is relatively new as a standard function, and certainly isn't part of standard three-terminal regulators. When present, shutdown control is a logic level controllable input, whereby a digital HIGH (or LO) is defined as regulation active (or vice-versa).

The error output, $\overline{ERR}$, is useful within a system to detect regulator overload, such as saturation of the pass device, thermal overload, etc. The remaining functions shown are always part of an IC power regulator.

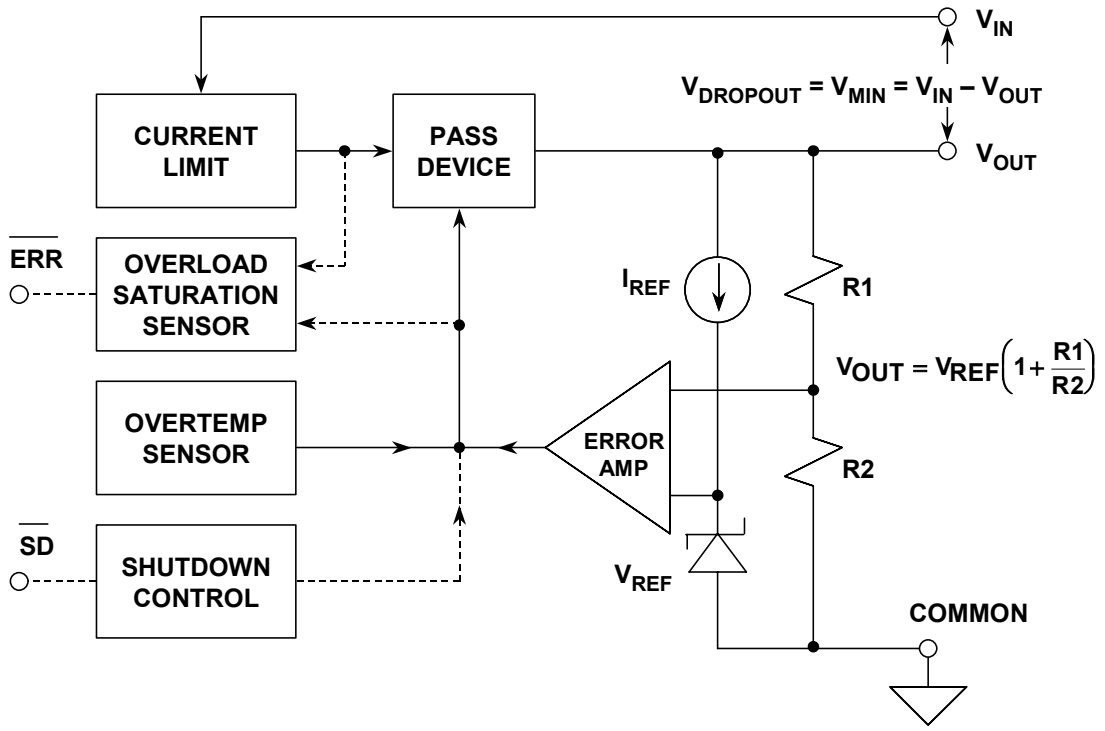


Figure 7.27: *Block Diagram of a Voltage Regulator*

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a bandgap based voltage, typically ~1.2 V, which allows output voltages of 3 V or more from supplies as low as 5 V. This voltage is presented to one input of an error amplifier, with the other input connected to the V_{OUT} sensing divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right). \qquad \text{Eq. 7.12}$$

With a typical bandgap reference voltage of 1.2 V, the R1/R2 ratio will be approximately 3/1 for a 5-V output. When standby power is critical, several design steps will be taken. The resistor values of the divider will be high, the error amplifier and pass device driver will be low power, and the reference current I_{REF} will also be low. By these means the regulator's unloaded standby current can be reduced to a mA or less using bipolar technology, and to only a few μA in CMOS parts. In regulators which offer a shutdown mode, the shutdown state standby current will be reduced to a μA or less.

Nearly all regulators will have some means of current limiting and over temperature sensing, to protect the pass device against failure. Current limiting is usually by a series sensing resistor for high current parts, or alternately by a more simple drive current limit to a controlled β pass device (which achieves the same end). For higher voltage circuits, this current limiting may also be combined with voltage limiting, to provide complete load line control for the pass device.

All power regulator devices will also have some means of sensing over-temperature, usually by means of a fixed reference voltage and a V_{BE}-based sensor monitoring chip temperature. When the die temperature exceeds a dangerous level (above ~150°C), this can be used to shutdown the chip, by removing the drive to the pass device. In some cases an error flag output may be provided to warn of this shutdown (and also loss of regulation from other sources).

Pass Devices and their Associated Tradeoffs

The discussion thus far has not treated the pass device in any detail. In practice, this major part of the regulator can actually take on quite a number of alternate forms. Precisely which type of pass device is chosen has a major influence on almost all major regulator performance issues. Most notable among these is the dropout voltage, V_{MIN}.

Figure 7.28a through 7.28e illustrates a number of pass devices which are useful within voltage regulator circuits, shown in simple schematic form. On the figure is also listed the salient V_{MIN} for the device as it would typically be used, which directly indicates its utility for use in an LDO. Not shown in these various mini-figures are the remaining circuits of a regulator.

It is difficult to fully compare all of the devices from their schematic representations, since they differ in so many ways beyond their applicable dropout voltages. For this reason, the chart of Figure 7.29 is useful.

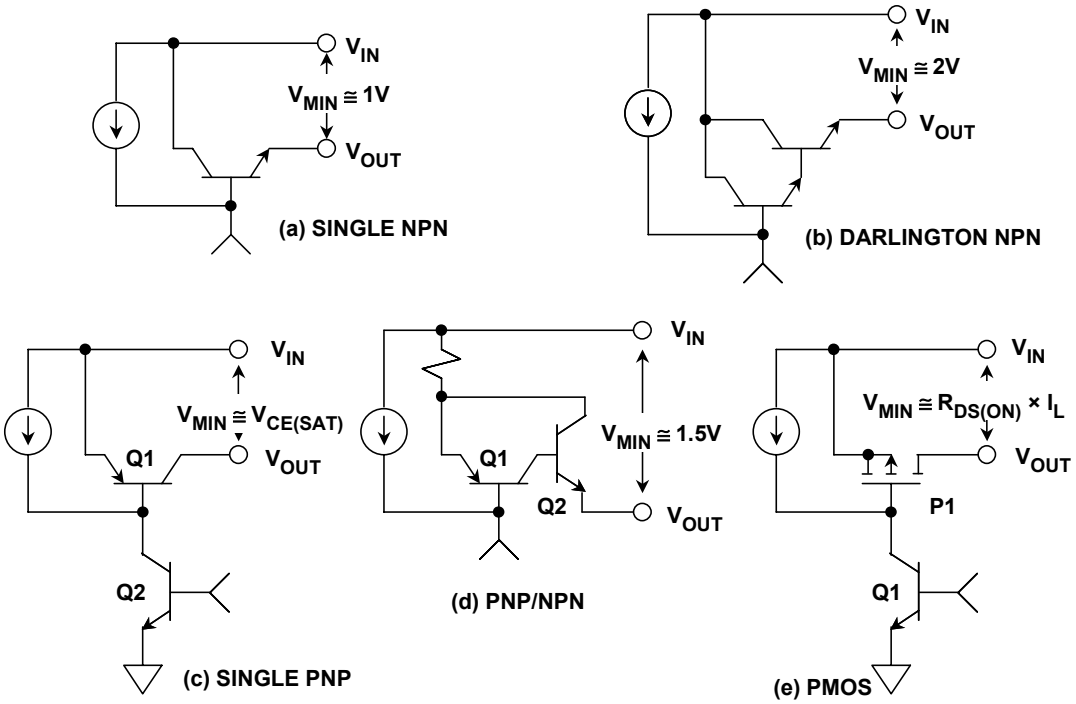


Figure 7.28: *Pass Devices Useful in Voltage Regulators*

A SINGLE NPN	B DARLINGTON NPN	C SINGLE PNP	D PNP/NPN	E PMOS
V_{MIN} ~ 1V	V_{MIN} ~ 2V	V_{MIN} ~ 0.1V	V_{MIN} ~ 1.5V	$V_{MIN} \sim R_{DS(ON)} \times I_L$
I_L < 1A	I_L > 1A	I_L < 1A	I_L > 1A	I_L > 1A
Follower	Follower	Inverter	Inverter	Inverter
Low Z_{OUT}	Low Z_{OUT}	High Z_{OUT}	High Z_{OUT}	High Z_{OUT}
Wide BW	Wide BW	Narrow BW	Narrow BW	Narrow BW
C_L Immune	C_L Immune	C_L Sensitive	C_L Sensitive	C_L Sensitive

Figure 7.29: *Pros and Cons of Voltage Regulator Pass Devices*

This chart compares the various pass elements in greater detail, allowing easy comparison between the device types, dependent upon which criteria is most important. Note that columns A-E correspond to the schematics of Figure 7.28a-7.28e. Note also that the pro/con comparison items are in *relative* terms, as opposed to a hard specification limit for any particular pass device type.

For example, it can be seen that the all NPN pass devices of columns A and B have the attributes of a follower circuit, which allows high bandwidth and provides relative immunity to cap loading because of the characteristic low Z_{OUT}. However, neither the single NPN nor the Darlington NPN can achieve low dropout, for any load current. This is because the V_{BE}(s) of the pass device appears in series with the input, preventing its saturation, and thus setting a V_{MIN} of about 1 or 2 V.

By contrast, the inverting mode device connections of both columns C and E do allow the pass device to be effectively saturated, which lowers the associated voltage losses to a minimum. This single factor makes these two pass device types optimum for LDO use, at least in terms of power efficiency.

For currents below 1 A, either a single PNP or a PMOS pass device is most useful for low dropout, and they both can achieve a V_{MIN} of 0.1 V or less at currents of 100 mA. The dropout voltage of a PNP will be highly dependent upon the actual device used and the operating current, with vertical PNP devices being superior for saturation losses, as well as minimizing the I_{ground} spike when in saturation. PMOS pass devices offer the potential for the lowest possible V_{MIN}, since the actual dropout voltage will be the product of the device $R_{DS(ON)}$ and I_L. Thus a low $R_{DS(ON)}$ PMOS device can always be chosen to minimize V_{MIN} for a given I_L. PMOS pass devices are typically *external* to the LDO IC, making the IC actually a controller (as opposed to a complete and integral LDO). PMOS pass devices can allow currents up to several amps or more with very low dropout voltages. The PNP/NPN connection of column D is actually a hybrid hookup, intended to boost the current of a single PNP pass device. This it does, but it also adds the

V_{BE} of the NPN in series (which cannot be saturated), making the net V_{MIN} of the connection about 1.5 V.

All of the three connections C/D/E have the characteristic of high output impedance, and require an output capacitor for stability. The fact that the output cap is part of the regulator frequency compensation is a most basic application point, and one which needs to be clearly understood by the regulator user. This factor, denoted by "C_L sensitive", makes regulators using them generally critical as to the exact C_L value, as well as its ESR (equivalent series resistance). Typically this type of regulator must be used only with a specific size as well as type of output capacitor, where the ESR is controlled with respect to both time and temperature to fully guarantee regulator stability. Fortunately, some recent Analog Devices LDO IC circuit developments have eased this burden on the part of the regulator user a great deal, and will be discussed below in further detail.

Some examples of standard IC regulator architectures illustrate the points above regarding pass devices, and allow an appreciation of regulator developments leading up to more recent LDO technologies.

The classic LM309 5-V/1-A three-terminal regulator (see Reference 1) was the originator in a long procession of regulators. This circuit is shown in much simplified form in Figure 7.30, with current limiting and over temperature details omitted. This IC type is still in standard production today, not just in original form, but in family derivatives such as the 7805, 7815 etc., and their various low and medium current alternates. Using a Darlington pass connection for Q18-Q19, the design has never been known for low dropout characteristics (~1.5-V typical), or for low quiescent current (~5 mA). It is however relatively immune to instability issues, due to the internal compensation of C1, and the buffering of the emitter follower output. This helps make it easy to apply.

The LM109/309 bandgap voltage reference actually used in this circuit consists of a more involved scheme, as opposed to the basic form which was described with Figure 7.3. Resistor R8 drops a PTAT voltage, which drives the Darlington connected error amplifier, Q9-Q10. The negative TC V_{BE}s of Q9-Q10 and Q12-Q13 are summed with this PTAT voltage, and this sum produces a temperature-stable 5-V output voltage. Current buffering of the error amplifier Q10 is provided by PNP Q11, which drives the NPN pass devices.

Later developments in references and three-terminal regulation techniques led to the development of the voltage adjustable regulator. The original IC to employ this concept was the LM317 (see Reference 2), which is shown in simplified schematic form in Figure 7.31. Note that this design does not use the same ΔV_{BE} form of reference as in the LM309. Instead, Q17-Q19, etc. are employed as a form of a Brokaw bandgap reference cell (see Figure 7.4 again, and Reference 3).

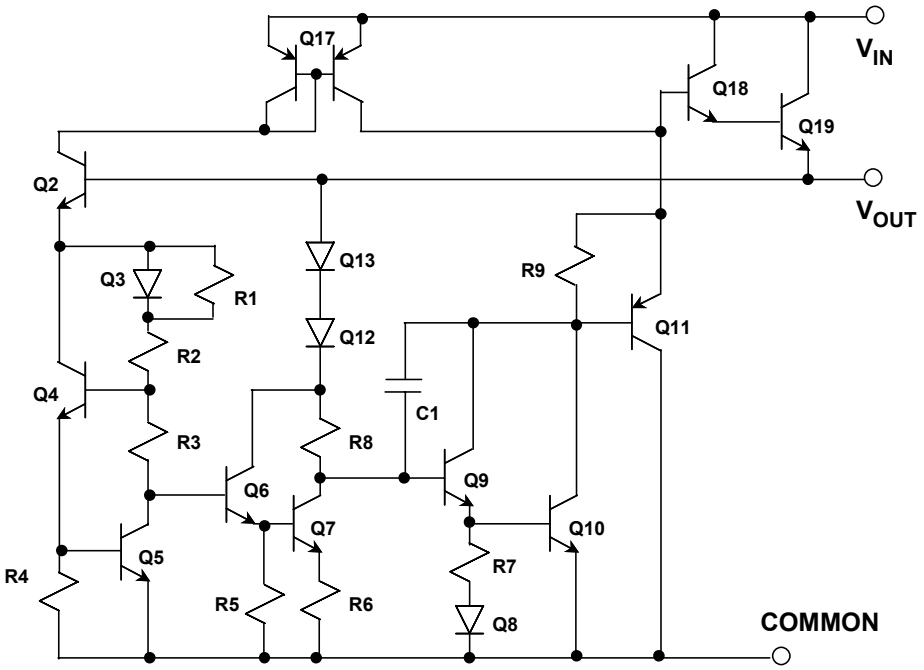


Figure 7.30: *Simplified Schematic of LM309 Fixed 5-V/1-A Three-Terminal Regulator*

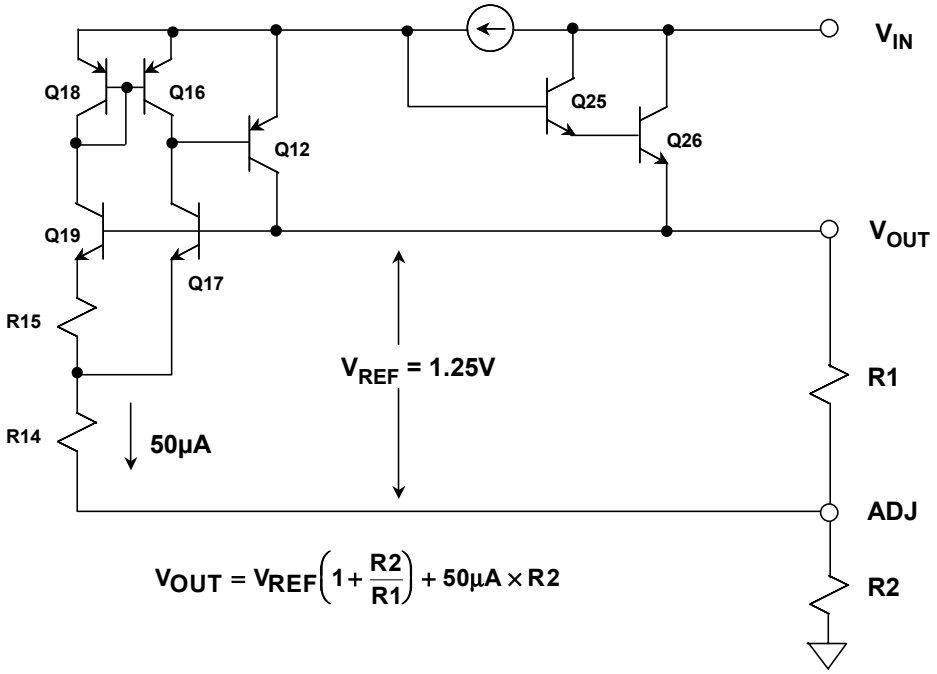


Figure 7.31: *Simplified Schematic of LM317 Adjustable Three-terminal Regulator*

This adjustable regulator bootstraps the reference cell transistors Q17-Q19 and the error amplifier transistors Q16-Q18. The output of the error amplifier drives Darlington pass transistors Q25-Q26, through buffer Q12. The basic reference cell produces a fixed voltage of 1.25 V, which appears between the V_{OUT} and ADJ pins of the IC as shown. External scaling resistors R1 and R2 set up the desired output voltage, which is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R2}{R1}\right) + 50\mu A \times R2 \,. \qquad \text{Eq. 7.13}$$

As can be noted, the voltage output is a scaling of V_{REF} by R2-R1, plus a small voltage component which is a function of the 50-μA reference cell current. Typically, the R1-R2 values are chosen to draw >5 mA, making the rightmost term relatively small by comparison. The design is internally compensated, and in many applications will not necessarily need an output bypass capacitor.

Like the LM309 fixed voltage regulator, the LM317 series has relatively high dropout voltage, due to the use of Darlington pass transistors. It is also not a low power IC (quiescent current typically 3.5 mA). The strength of this regulator lies in the wide range of user voltage adaptability it allows.

Subsequent variations on the LM317 pass device topology modified the method of output drive, substituting a PNP/NPN cascade for the LM317's Darlington NPN pass devices. This development achieves a lower V_{MIN}, 1.5 V or less (see Reference 4). The modification also allows all of the general voltage programmability of the basic LM317, but at some potential increase in application sensitivity to output capacitance. This sensitivity is brought about by the fundamental requirement for an output capacitor for the IC's frequency compensation, which is a differentiation from the original LM317.

Low Dropout Regulator Architectures

As has been shown thus far, all LDO pass devices have the fundamental characteristics of operating in an inverting mode. This allows the regulator circuit to achieve pass device saturation, and thus low dropout. A by-product of this mode of operation is that this type of topology will necessarily be more susceptible to stability issues. These basic points give rise to some of the more difficult issues with regard to LDO performance. In fact, these points influence both the design and the application of LDOs to a very large degree, and in the end, determine how they are differentiated in the performance arena.

A traditional LDO architecture is shown in Figure 7.32, and is generally representative of actual parts employing either a PNP pass device as shown, or alternately, a PMOS device. There are both dc and ac design and application issues to be resolved with this architecture, which are now discussed.

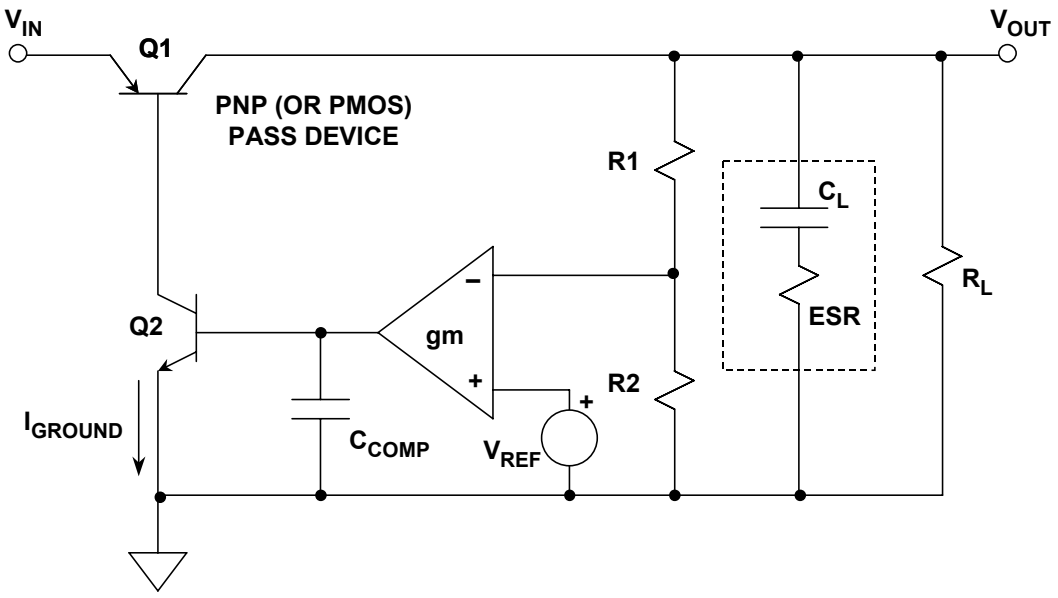


Figure 7.32: *Traditional LDO Architecture*

In dc terms, perhaps the major issue is the type of pass device used, which influences dropout voltage and ground current. If a lateral PNP device is used for Q1, the β will be low, sometimes only on the order or 10 or so. Since Q1 is driven from the collector of Q2, the relatively high base current demanded by a lateral PNP results in relatively high emitter current in Q2, or a high I_{ground}. For a typical lateral PNP based regulator operating with a 5-V/150-mA output, I_{ground} will be typically ~18 mA, and can be as high as 40 mA. To compound the problem of high I_{ground} in PNP LDOs, there is also the "spike" in I_{ground}, as the regulator is operating within its dropout region. Under such conditions, the output voltage is out of tolerance, and the regulation loop forces higher drive to the pass device, in an attempt to maintain loop regulation. This results in a substantial spike upward in I_{ground}, which is typically internally limited by the regulator's saturation control circuits.

PMOS pass devices do not demonstrate a similar current spike in I_{ground}, since they are voltage controlled. But, while devoid of the I_{ground} spike, PMOS pass devices do have some problems of their own. Problem number one is that high quality, low R_{ON}, low threshold PMOS devices generally aren't compatible with many IC processes. This makes the best technical choice for a PMOS pass device an external part, driven from the collector of Q2 in the figure. This introduces the term "LDO controller", where the LDO architecture is completed by an external pass device. While in theory NMOS pass devices would offer lower R_{ON} choice options, they also demand a boosted voltage supply to turn on, making them impractical for a simple LDO. PMOS pass devices are widely available in low both R_{ON} and low threshold forms, with current levels up to several amperes. They offer the potential of the lowest dropout of any device, since dropout can always be lowered by picking a lower R_{ON} part.

The dropout voltage of lateral PNP pass devices is reasonably good, typically around 300 mV at 150 mA, with a maximum of 600 mV. These levels are however considerably bettered in regulators using vertical PNPs, which have a typical β of ~150 at currents of 200 mA. This leads directly to an I_{ground} of 1.5 mA at the 200-mA output current. The

dropout voltage of vertical PNPs is also an improvement vis-à-vis that of the lateral PNP regulator, and is typically 180 mV at 200 mA, with a maximum of 400 mV.

There are also major ac performance issues to be dealt with in the LDO architecture of Figure. 7.32. This topology has an inherently high output impedance, due to the operation of the PNP pass device in a common-emitter (or common-source with a PMOS device) mode. In either case, this factor causes the regulator to appear as a high source impedance to the load.

The internal compensation capacitor of the regulator, C_{COMP}, forms a fixed frequency pole, in conjunction with the g_m of the error amplifier. In addition, load capacitance C_L forms an output pole, in conjunction with R_L. This particular pole, because it is a second (and sometimes variable) pole of a two-pole system, is the source of a major LDO application problem. The C_L pole can strongly influence the overall frequency response of the regulator, in ways that are both useful as well as detrimental. Depending upon the relative positioning of the two poles in the frequency domain, along with the relative value of the ESR of capacitor C_L, it is quite possible that the stability of the system can be compromised for certain combinations of C_L and ESR. Note that C_L is shown here as a real capacitor, which is actually composed of a pure capacitance plus the series parasitic resistance ESR.

Without a heavy duty exercise into closed-loop stability analysis, it can safely be said that LDOs, like other feedback systems, need to satisfy certain basic stability criteria. One of these is the gain-versus-frequency rate-of-change characteristic in the region approaching the system's unity loop gain crossover point. For the system to be closed loop stable, the phase shift must be less than 180° at the point of unity gain. In practice, a good feedback design needs to have some phase margin, generally 45° or more to allow for various parasitic effects. While a single pole system is intrinsically stable, two pole systems are *not* necessarily so—they may in fact be stable, or they may also be unstable. Whether or not they are stable for a given instance is highly dependent upon the specifics of their gain-phase characteristics.

If the two poles of such a system are widely separated in terms of frequency, stability may not be a serious problem. The emitter-follower output of a classic regulator like the LM309 is an example with widely separated pole frequencies, as the very low Z_{OUT} of the NPN follower pushes the output pole due to load capacitance far out in frequency, where it does little harm. The internal compensation capacitance (C1 of Fig. 7.30, again) then forms part of a *dominant pole*, which reduces loop gain to below unity at the much higher frequencies where the output pole does occur. Thus stability is not necessarily compromised by load capacitance in this type of regulator.

Figure 7.33 summarizes the various dc and ac design issues of LDOs.

DC	AC
◆ Lateral PNP Pass Device: High I_{GROUND}	◆ Two Pole Compensation System
◆ Vertical PNP Pass Device: Low I_{GROUND} Low V_{MIN}	◆ C_L ESR Critical to Stability
	◆ Requires Large C_L
◆ PMOS Pass Device: Lowest I_{GROUND} Variation Low V_{MIN} Ampere Level Output Currents	◆ Requires"Zoned" C_L ESR (Max/Min ESR Limits Over Time and Temperature)

Figure 7.33: *DC and AC Design Issues in Low Dropout Regulators*

By their nature however, LDOs simply can't afford the luxury of emitter follower outputs, they must instead operate with pass devices capable of saturation. Thus, given the existence of two or more poles (one or more internal and a second formed by external loading) there is the potential for the cumulative gain-phase to add in a less than satisfactory manner. The potential for instability under certain output loading conditions is, for better or worse, a fact-of-life for most LDO topologies.

However, the output capacitor which gives rise to the instability can, for certain circumstances, also be the solution to the same instability. This seemingly paradoxical situation can be appreciated by realizing that almost all practical capacitors are actually as shown in Fig. 7.32, a series combination of the capacitance C_L and a parasitic resistance, ESR. While load resistance R_L and C_L do form a pole, C_L and its ESR also form a zero. The effect of the zero is to mitigate the de-stabilizing effect of C_L for certain conditions.

For example, if the pole and zero in question are appropriately placed in frequency relative to the internal regulator poles, some of the deleterious effects can be made to essentially cancel, leaving little or no problematic instability (see Reference 5). The basic problem with this setup is simply that the capacitor's ESR, being a parasitic term, is not at all well controlled. As a result, LDOs which depend upon output pole-zero compensation schemes must very carefully limit the capacitor ESR to certain *zones*, such as shown by Figure 7.34.

A zoned ESR chart such as this is meant to guide the user of an LDO in picking an output capacitor which confines ESR to the stable region, i.e., the central zone, for all operating conditions. Note that this generic chart is not intended to portray any specific device, just the general pattern. Unfortunately, capacitor facts of life make such data somewhat limited in terms of the real help it provides. Bearing in mind the requirements of such a zoned chart, it effectively means that general purpose aluminum electrolytic are prohibited from use, since they deteriorate in terms of ESR at cold temperatures. Very low ESR types such as OS-CON or multi-layer ceramic units have ESRs which are too low for use. While they could in theory be padded up into the stable zone with external resistance, this would hardly be a practical solution. This leaves tantalum types as the best all around choice for LDO output use. Finally, since a large capacitor value is likely to be used to maximize stability, this effectively means that the solution for an LDO such as Fig. 7.32 must use a more expensive and physically large tantalum capacitor. This is not desirable if small size is a major design criteria.

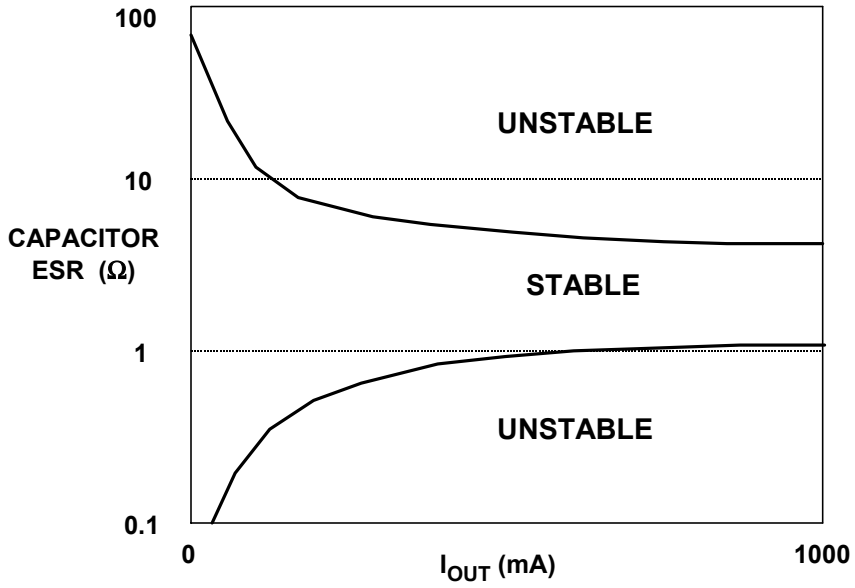


Figure 7.34: *Zoned Load Capacitor ESR Can Make an LDO Applications Nightmare*

The anyCAP® Low Dropout Regulator Family

Some novel modifications to the basic LDO architecture of Fig. 7.32 allow major improvements in terms of both dc and ac performance. These developments are shown schematically in Figure 7.35, which is a simplified diagram of the Analog Devices ADP330x, and ADP333x-series LDO regulator family. These regulators are also known as the anyCAP® family, so named for their relative insensitivity to the output capacitor in terms of both size and ESR. They are available in power efficient packages such as the Thermal Coastline (discussed below), in both stand-alone LDO and LDO controller forms, and also in a wide span of output voltage options.

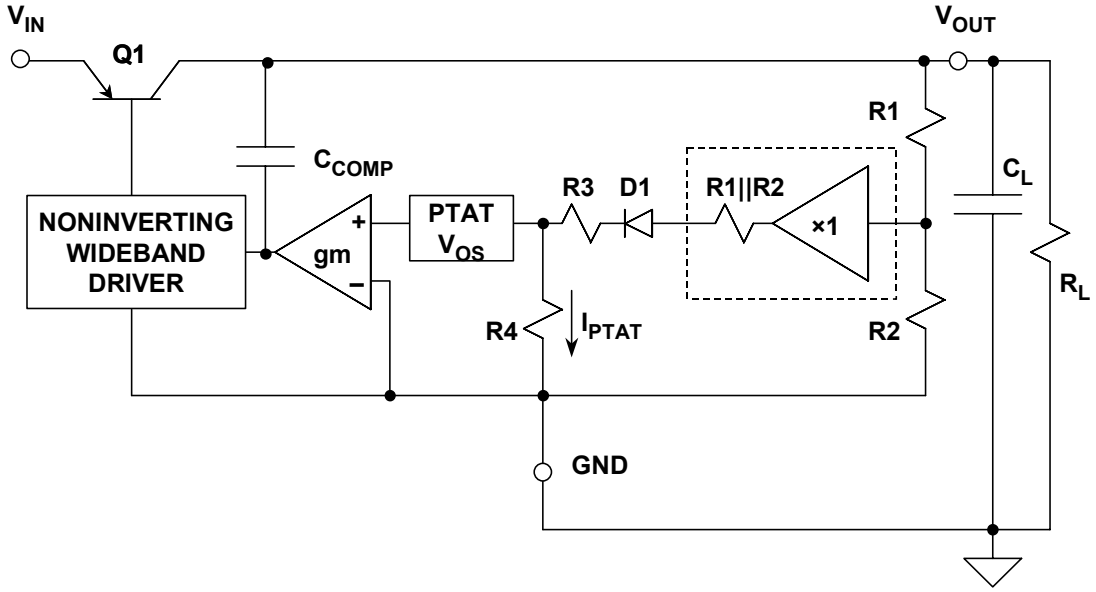


Figure 7.35: *ADP330x and ADP333x anyCAP® Topology Features Improved DC & AC Performance Over Traditional LDOs*

Design Features Related to DC Performance

One of the key differences in the ADP330x/ADP333x-series is the use of a high gain vertical PNP pass device, with all of the advantages described above with Figs. 7.32 and 7.33 (also, see Reference 6). This allows the typical dropout voltages for the series to be on the order of 1 mV/mA for currents of 200 mA or less.

It is important to note that the topology of this LDO is distinctly different from that of the generic form in Fig. 7.32, as there is no obvious V_{REF} block. The reason for this is the fact that the ADP330x/ADP333x-series uses what is termed a "merged" amplifier-reference design. The operation of the integral amplifier and reference scheme illustrated in Fig. 7.35 can be described as follows.

In this circuit, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1||R2, then actual components D1, R3, R4, etc.

The error amplifier, shown here as a gm stage, is actually a PNP input differential stage with the two transistors of the pair operated at different current densities, so as to produce a predictable PTAT offset voltage. Although shown here as a separate block V_{OS}, this offset voltage is inherent to a bipolar pair for such operating conditions. The PTAT V_{OS} causes a current I_{PTAT} to flow in R4, which is simply:

$$I_{PTAT} = \frac{V_{OS}}{R4}. \qquad \text{Eq. 7.14}$$

Note that this current also flows in series connected R4, R3, and the Thevenin resistance of the divider, R1||R2, so:

$$V_{PTAT} = I_{PTAT}(R3 + R4 + R1 \,||\, R2). \quad \text{Eq. 7.15}$$

The *total* voltage defined as V_{REF} is the sum of two component voltages:

$$V_{REF} = V_{PTAT} + V_{D1}, \quad \text{Eq. 7.16}$$

where the I_{PTAT} scaled voltages across R3, R4, and R1||R2 produce a net PTAT voltage V_{PTAT}, and the diode voltage V_{D1} is a CTAT voltage. As in a standard bandgap reference, the PTAT and CTAT components add up to a temperature stable reference voltage of 1.25 V. In this case however, the reference voltage is not directly accessible, but instead it exists in the virtual form described above. It acts as it would be seen at the output of a zero impedance divider of a numeric ratio of R1/R2, which is then fed into the R3-D1 series string through a Thevenin resistance of R1||R2 in series with D1.

With the closed loop regulator at equilibrium, the voltage at the virtual reference node will be:

$$V_{REF} = V_{OUT}\left(\frac{R2}{R1 + R2}\right). \quad \text{Eq. 7.17}$$

With minor re-arrangement, this can be put into the standard form to describe the regulator output voltage, as:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right). \quad \text{Eq. 7.18}$$

In the various devices of the ADP330x/ADP333x-series, the R1-R2 divider is adjusted to produce various standard output voltages from 1.5 V to 5.0 V.

As can be noted from this discussion, unlike a conventional reference setup, there is no power wasting reference current such as used in a conventional regulator topology (I_{REF} of Fig. 7.27). In fact, the Fig. 7.35 regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

Design Features Related to AC Performance

While the above described dc performance enhancements of the ADP330x series are worthwhile, the most dramatic improvements come in areas of ac-related performance. These improvements are in fact the genesis of the anyCAP® series name.

Capacitive loading and the potential instability it brings is a major deterrent to easily applying LDOs. While low dropout goals prevent the use of emitter follower type outputs, and so preclude their desirable buffering effect against cap loading, there is an alternative technique of providing load immunity. One method of providing a measure

of insusceptibility against variation in a particular amplifier response pole is called *pole splitting* (see Reference 8). It refers to an amplifier compensation method whereby two response poles are shifted in such a way so as to make one a dominant, lower frequency pole. In this manner the secondary pole (which in this case is the C_L related output pole) becomes much less of a major contributor to the net ac response. This has the desirable effect of greatly de-sensitizing the amplifier to variations in the output pole.

A Basic Pole-Splitting Topology

A basic LDO topology with frequency compensation as modified for pole splitting is shown in Figure 7.36. Here the internal compensation capacitor C_{COMP} is connected as an integrating capacitor, around pass device Q1 (C1 is the pass device input capacitance). While it is true that this step will help immunize the regulator to the C_L related pole, it also has a built in fatal flaw. With C_{COMP} connected directly to the Q1 base as shown, the line rejection characteristics of this setup will be quite poor. In effect, when doing it this way one problem (C_L sensitivity) will be exchanged for another (poor line rejection).

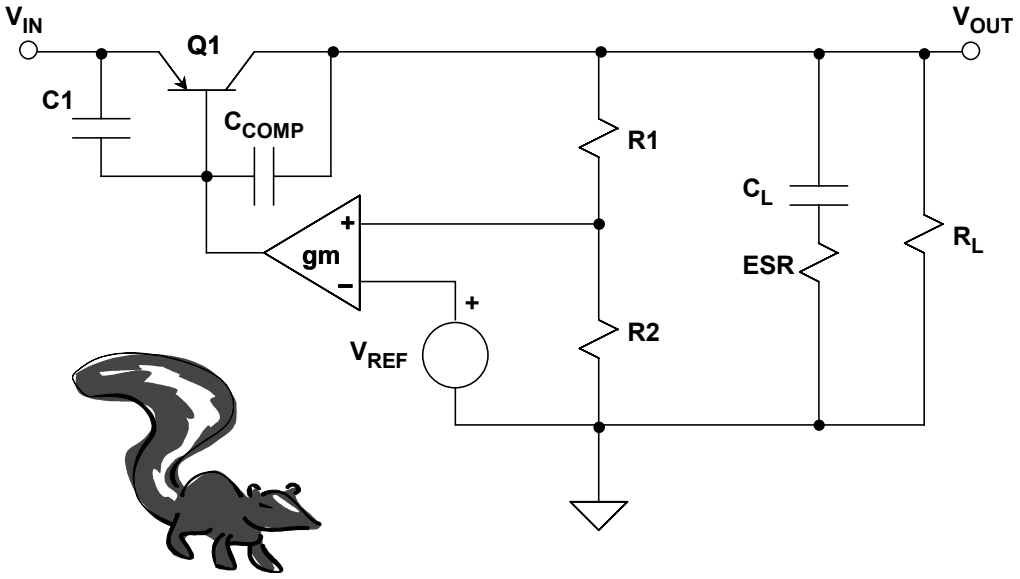


Figure 7.36: *The Solution to CL Sensitivity: Pole Split Compensation (Wrong Way Example!)*

The anyCAP® Pole-Splitting Topology

Returning to the anyCAP series topology, (Fig. 7.35, again) it can be noted that in this case C_{COMP} is isolated from the pass device's base (and thus input ripple variations), by the wideband non-inverting driver. But insofar as frequency compensation is concerned, because of this buffer's isolation, C_{COMP} still functions as a modified pole splitting capacitor (see Reference 9), and it does provide the benefits of a buffered, C_L independent single-pole response. The regulator's frequency response is dominated by the internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L. Thus the name anyCAP for the series is apt, as the design is tolerant of virtually any output capacitor type.

The benefits of the anyCAP topology are summarized by Figure 7.37. As can be noted, C_L can be as low as 0.47 µF, and it can also be a multi-layer ceramic capacitor (MLCC) type. This allows a very small physical size for the entire regulation function, such as when a SOT-23 packaged anyCAP LDO is used, for example the ADP3300 device. Because of the in-sensitivity to C_L, the designer needn't worry about such things as ESR zones, and can better concentrate on the system aspects of the regulator application.

- **Internal C_{COMP} Dominates Response Rolloff**
- **C_L Can Range from 0.47µF(min) to Infinity**
- **Low and Ultra-Low C_L ESR is OK**
- **MLCC Types for C_L Work, is Physically Smallest Solution**
- **No ESR Exclusion Zones**
- **Fast Load Transient Response and Good Line Rejection**

Figure 7.37: *Benefits of anyCAP® LDO Topology*

The anyCAP® LDO series devices

The major specifications of the ADP330x-series anyCAP LDO regulators are summarized in Figure. 7.38. The devices include both single and dual output parts, with current capabilities ranging from 50 to 200 mA. Rather than separate individual specifications for output tolerance, line and load regulation, plus temperature, the anyCAP series devices are rated simply for a combined total accuracy figure. For the ADP3300, ADP3301, ADP3302, ADP3303, and ADP3307, this accuracy is either 0.8% at 25°C, or 1.4% over the temperature range with the device operating over an input range of V_{OUT} +0.3 V (or 0.5 V), up to 12 V. The ADP3308 and ADP3309 are similarly specified for a total 25°C accuracy of 1.1% and 2.2% over temperature. With total accuracy being covered by one clear specification, the designer can then achieve a higher degree of confidence. It is important to note that this method of specification also includes operation within the regulator dropout range (unlike some LDO parts specified for higher input-output voltage difference conditions).

The ADP333x-series are a newer family of anyCAP LDOs designed for 200-mA and higher output currents with very low quiescent current, I_Q. For instance, the ADP3330 has a typical no-load current of only 35 µA. The ADP333x-series are available in thermally enhanced packages, and Figure 7.39 shows the key specifications for the family.

Part Number	V_{MIN} @ I_L (V, typ)	I_L (mA)	Accuracy (Total over Temp, %)	Package (All SO-8 are Thermal coastline)	Comment (Singles have NR, SD, ERR; Dual no NR)
ADP3300	0.08	50	1.4	SOT-23-6	Single
ADP3301	0.10	100	1.4	SO-8	Single
ADP3302	0.10	100	1.4	SO-8	Dual
ADP3303	0.18	200	1.4	SO-8	Single
ADP3307	0.13	100	1.4	SOT-23-6	Single
ADP3308	0.08	50	2.2	SOT-23-5	Single
ADP3309	0.12	100	2.2	SOT-23-5	Single

Figure 7.38: *anyCAP® Series LDO Regulators*

Part Number	V_{MIN} @ I_L (V, typ)	I_L (mA)	Accuracy (Total over Temp, %)	Package (SOT23-6 are Chip on Lead)	Comment
ADP3330	0.14	200	1.4	SOT-23-6	Single
ADP3331	0.14	200	1.4	SOT-23-6	Single
ADP3333	0.14	300	1.8	MSOP-8	Single
ADP3334	0.20	500	1.8	SO-8	Single
ADP3335	0.20	500	1.8	MSOP-8	Single
ADP3336	0.20	500	1.8	MSOP-8	Single
ADP3338	0.19	1000	1.4	SOT-223	Single
ADP3339	0.23	1500	1.5	SOT-223	Single

Figure 7.39: *anyCAP® Series Low I_Q LDOs*

Functional Diagram and Basic 50-mA LDO Regulator

A functional diagram common to the various devices of the anyCAP series LDO regulators is shown by Figure 7.40. Operation of the various pins and internal functions is discussed below.

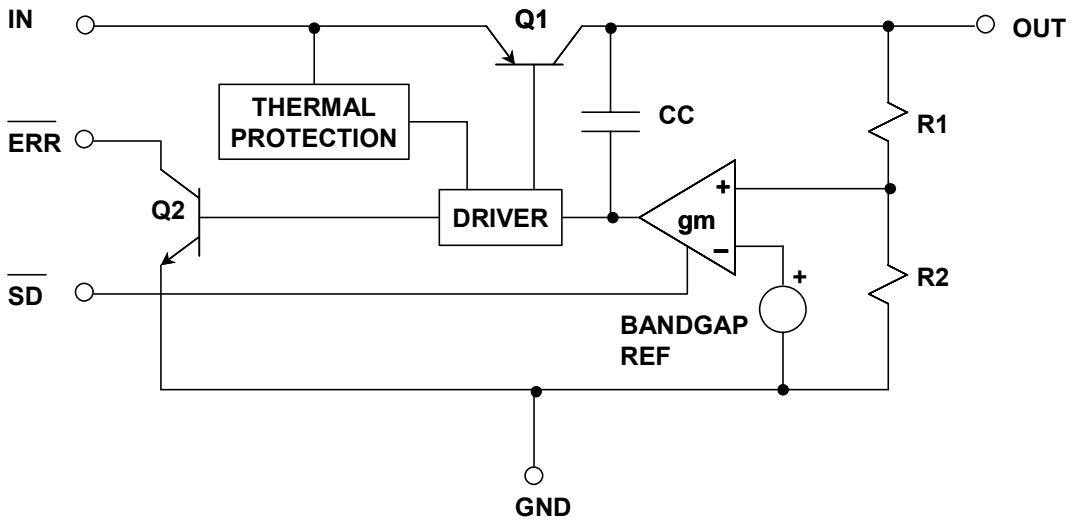


Figure 7.40: *anyCAP® Series LDO Regulators Functional Diagram*

In application, the use of the anyCAP series of LDOs is simple, as shown by a basic 50-mA ADP3300 regulator, in Figure 7.41. This circuit is a general one, to illustrate points common to the entire device series. The ADP3300 is a basic LDO regulator device, designed for fixed output voltage applications while operating from sources over a range of 3 to 12 V and a temperature range of –40°C to +85°C. The actual ADP3300 device ordered would be specified as ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for those respective voltages. The "ART" portion of the part number designates the SOT-23 6-lead package. The example circuit shown produces 5.0 V with the use of the ADP3300-5.

In operation, the circuit will produce its rated 5 V output for loads of 50 mA or less, and for input voltages above 5.3 V (V_{OUT} + 0.3 V), when the shutdown ($\overline{SD}$) input is in a HIGH state. This can be accomplished either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN}. When $\overline{SD}$ is LOW (or tied to ground), the regulator shuts down, and draws a quiescent current of 1 μA or less.

The ADP3300 and other anyCAP series devices maintain regulation over a wide range of load, input voltage and temperature conditions. However, when the regulator is overloaded or entering the dropout region (for example, by a reduction in the input voltage) the open collector $\overline{ERR}$ pin becomes active, by going to a LOW or conducting state. Once set, the $\overline{ERR}$ pin's internal hysteresis keeps the output low, until some

margin of operating range is restored. In the circuit of Fig. 7.41, R1 is a pullup resistor for the $\overline{ERR}$ output, E_{OUT}. This resistor can be eliminated if the load being driven provides a pullup current.

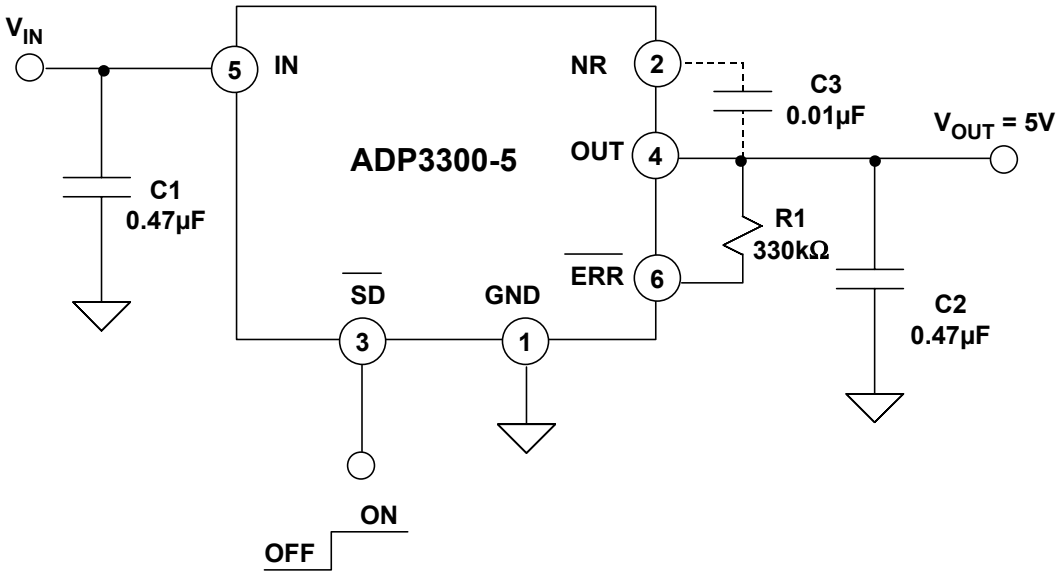


Figure 7.41: *A Basic ADP3300 50-mA LDO Regulator Circuit*

The $\overline{ERR}$ function can also be activated by the regulator's over temperature protection circuit, which trips at 165°C. These internal current and thermal limits are intended to protect the device against accidental overload conditions. For normal operation, device power dissipation should be externally limited by means of heat sinking, air flow, etc. so that junction temperatures will not exceed 125°C.

A capacitor, C3, connected between pins 2 and 4, can be used for an optional noise reduction (NR) feature. This is accomplished by ac-bypassing a portion of the regulator's internal scaling divider, which has the effect of reducing the output noise ~10 dB. When this option is exercised, only low leakage 10- to 100-nF capacitors should be used. Also, input and output capacitors should be changed to 1- and 4.7-µF values respectively, for lowest noise and the best overall performance. Note that the noise reduction pin is internally connected to a high impedance node, so connections to it should be carefully done to avoid noise. PC traces and pads connected to this pin should be as short and small as possible.

LDO Regulator Thermal Considerations

To determine a regulator's power dissipation, calculate it as follows:

$$P_D = (V_{IN} - V_{OUT})(I_L) + (V_{IN})(I_{ground}), \qquad \text{Eq. 7.19}$$

where I_L and I_{ground} are load and ground current, and V_{IN} and V_{OUT} are the input and output voltages respectively. Assuming I_L= 50 mA, I_{ground} = 0.5 mA, V_{IN} = 8 V, and V_{OUT} = 5 V, the device power dissipation is:

$$P_D = (8 - 5)(0.05) + (8)(0.0005) = 0.150 + .004 = 0.154 \text{ W}. \quad \text{Eq. 7.20}$$

To determine the regulator's temperature rise, ΔT, calculate it as follows (assume the θ_{JA} of the regulator is 165°C/W):

$$\Delta T = T_J - T_A = P_D \times \theta_{JA} = 0.154\text{W} \times 165°\text{C/W} = 25.4°\text{C}. \quad \text{Eq. 7.21}$$

With a maximum junction temperature of 125°C, this yields a calculated maximum safe ambient operating temperature of 125°C – 25.4°C, or just under 100°C. Since this temperature is in excess of the device's rated temperature range of 85°C, the device will then be operated conservatively at an 85°C (or less) maximum ambient temperature.

These general procedures can be used for other devices in the series, substituting the appropriate θ_{JA} for the applicable package, and applying the remaining operating conditions. For reference, a complete tutorial section on thermal management is contained in Chapter 9.

In addition, layout and PCB design can have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads, to transfer heat away from the package. Appropriate PC layout techniques should then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance in SOT-23 and SO-8 packages:

1. *PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the uppermost side of the PCB.*

2. *Electrically connect dual V_{IN} and V_{OUT} pins in parallel, as well as to the corresponding V_{IN} and V_{OUT} large area PCB lands.*

3. *In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.*

4. *Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).*

5. *Do not use solder mask or silkscreen on the heat dissipating traces, as they increase the net thermal resistance of the mounted IC package.*

A real life example visually illustrates a number of the above points far better than words can do, and is shown in Figure 7.42, a photo of the ADP3300 1.5" square evaluation PCB. The boxed area on the board represents the actual active circuit area.

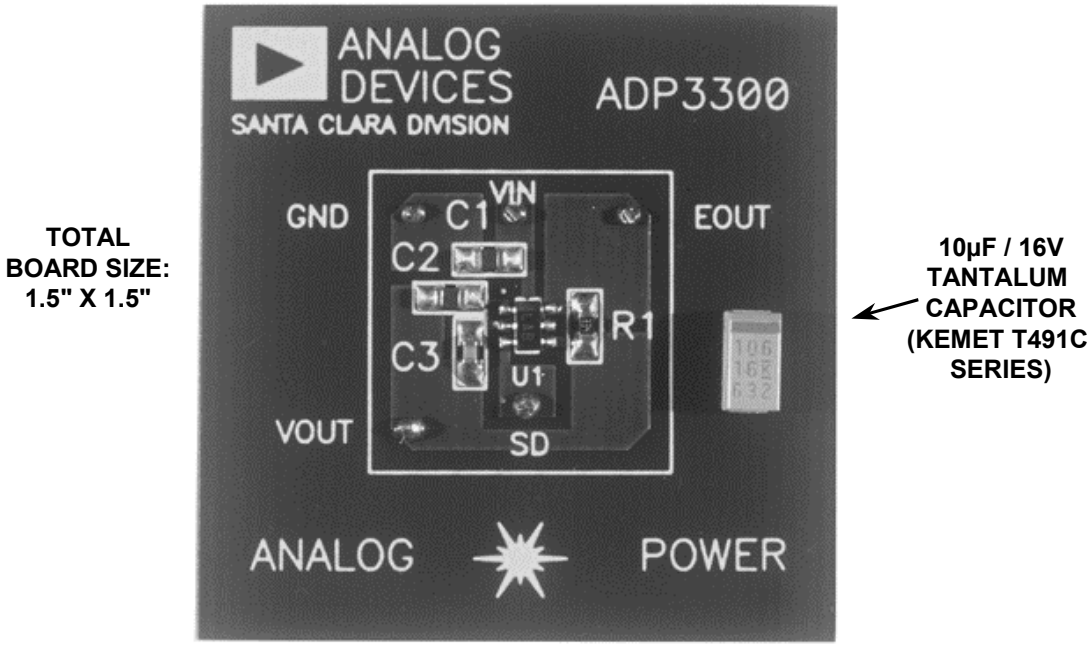


Figure 7.42: *ADP3300 Evaluation Board: Capacitor Size Can Make a Difference!*

In this figure, a large cross section conductor area can be seen associated with pin 4 and V_{OUT}, the large "U" shaped trace at the lower part within the boxed outline.

Also, the effect of the anyCAP design on capacitor size can be noted from the tiny size of the C1 and C2 0.47-µF input and output capacitors, near the upper left of the boxed area. For comparison purposes, a 10-µF/16-V tantalum capacitor (Kemet T491C-series) is also shown outside the box, as it might be used on a more conventional LDO circuit. It is several times the size of output capacitor C2.

Recent developments in packaging have led to much improved thermal performance for power management ICs. The anyCAP LDO regulator family capitalizes on this most effectively, using a thermally improved leadframe as the basis for all 8 pin devices. This package is called a "Thermal Coastline" design, and is shown in Figure 7.43. The foundation of the improvement in heat transfer is related to two key parameters of the leadframe design, distance and width. The payoff comes in the reduced thermal resistance of the leadframe based on the Thermal Coastline, only 90°C/W versus 160°C/W for a standard SO-8 package. The increased dissipation of the Thermal Coastline allows the anyCAP series of SO-8 regulators to support more than one watt of dissipation at 25°C.

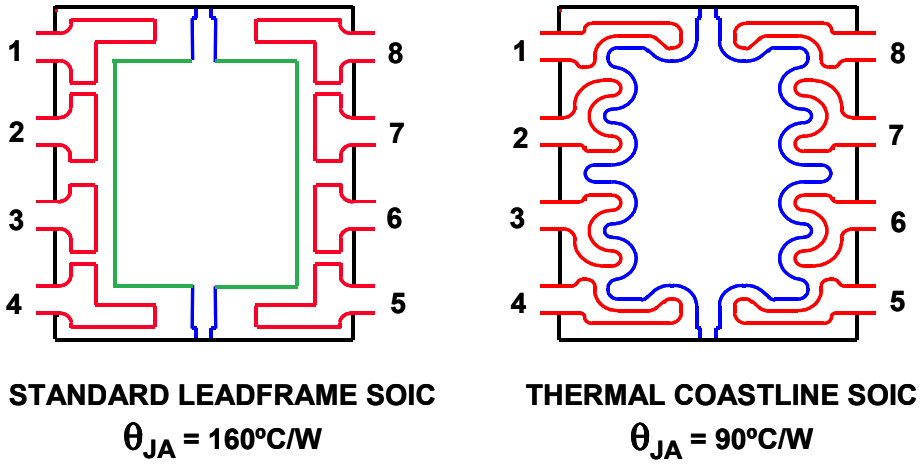


Figure 7.43: *anyCAP® Series Regulators in SO-8 Use Thermal Coastline Packages*

Additional insight into how the new leadframe increases heat transfer can be appreciated by Figure. 7.44. In this figure, it can be noted how the spacing of the Thermal Coastline paddle and leads shown on the right is reduced, while the width of the lead ends are increased, versus the standard leadframe, on the left.

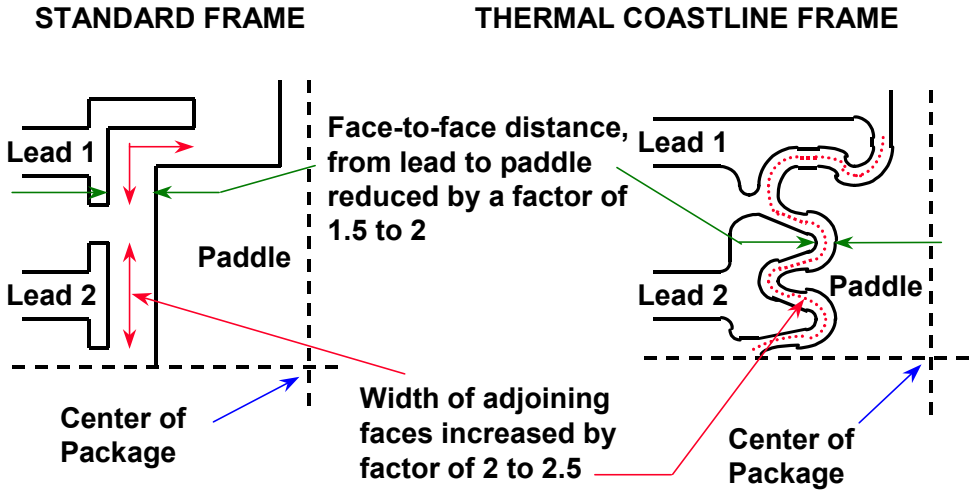
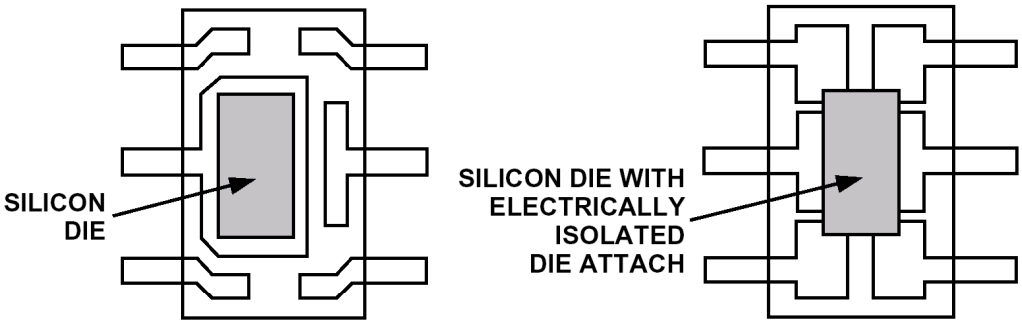


Figure 7.44: *Details of Thermal Coastline Package*

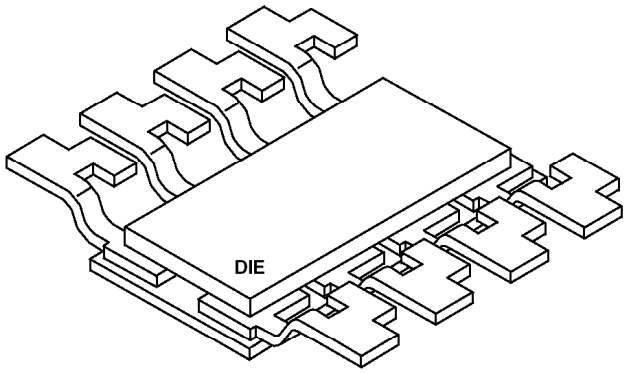
The ADP3330 and ADP3331 are 200-mA anyCAP LDOs packaged in a 6-lead SOT-23 package which utilizes a proprietary Chip-on-Lead™ packaging technique for thermal enhancement. In a standard SOT-23, the majority of the heat flows out of the ground pin. This new package uses an electrically isolated die attach that allows all pins to contribute to heat conduction. This technique reduces the thermal resistance to 165°C/W on a 4-layer board as compared to >230°C/W for a standard SOT-23 leadframe. Figure 7.45 shows the difference between the standard SOT-23 and the Chip-on-Lead leadframes.



165°C/W vs. >230°C/W for Standard SOT-23

Figure 7.45: *Thermally Enhanced Chip-on-Lead™ SOT-23-6 Package*

The ADP3333 (300 mA), ADP3335 (500 mA) and ADP3336 (500 mA) anyCAP LDOs use a patented "paddle-under-lead" package design to ensure the best thermal performance in an MSOP-8 footprint. This package uses an electrically isolated die attach that allows all pins to contribute to heat conduction. This technique reduces the thermal resistance to 110°C/W on a 4-layer board as compared to >160°C/W for a standard MSOP-8 leadframe. Figure 7.46 shows the standard physical construction of the MSOP-8 (left) and the thermally enhanced paddle-under-lead leadframe (right).



110°C/W vs. >160°C/W for Standard MSOP-8

Figure 7.46: *Thermally Enhanced "Paddle-Under-Lead" 8-Lead MSOP Package*

The ADP3338 (1 A) and ADP3339 (1.5 A) anyCAP LDOs are packaged in a thermally enhanced SOT-223 package as shown in Figure 7.47. The SOT-223's thermal resistance, θ_{JA}, is determined by the sum of the junction-to-case and the case-to-ambient thermal resistances. The junction-to-case thermal resistance, θ_{JC}, is determined by the package design and specified at 26.8°C/W. However, the case-to-ambient thermal resistance is determined by the printed circuit board design. As shown in Figure 7.47A-C, the amount of copper the ADP3338/ADP3339 is mounted to affects the thermal performance. When mounted to 2 oz. copper with just the minimal pads (Figure 7.47A), the θ_{JA} is 126.6°C/W.

By adding a small copper pad under the ADP3338 (Figure 7.47B), the θ_{JA} is reduced to 102.9°C/W. Increasing the copper pad to 1 square inch (Figure 7.47C), reduces the θ_{JA} even further to 52.8°C/W. Note that both pin 2 and pin 4 (tab) are the LDO output and are internally connected.

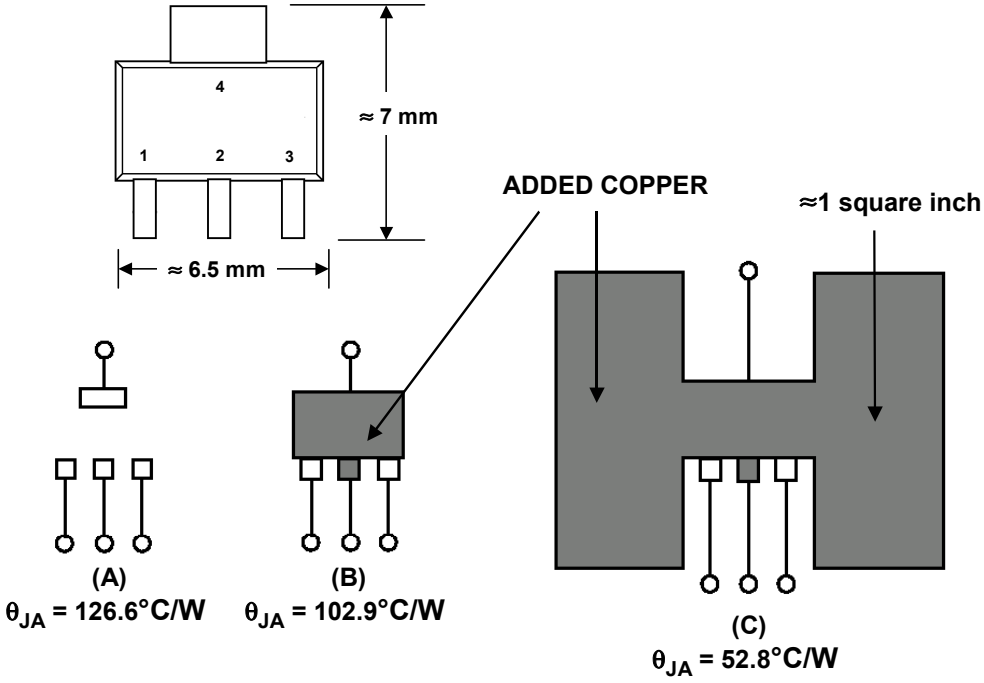


Figure 7.47: *Reducing SOT-223 Package θ_{JA}*

LDO Regulator Controllers

To complement the anyCAP series of standalone LDO regulators, there is also the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator IC is no longer useful in either load current or power dissipation terms, and uses an external PMOS FET for the pass device. The ADP3310 is a basic LDO regulator controller device, designed for fixed output voltage applications while operating from sources over a range of 3.8 to 15 V and a temperature range of –40 to +85°C. The actual ADP3310 device ordered would be specified as ADP3310AR-YY, where the "YY" is a voltage designator suffix such as 2.8, 3, 3.3, or 5, for those respective voltages. The "AR" portion of the part number designates the SO-8 Thermal Coastline 8-lead package. A summary of the main features of the ADP3310 device is listed in Figure 7.48.

- **Controller drives external PMOS power FETs**
  - **User FET choice determines I_L and V_{MIN} performance**
  - **Small, 2 chip regulator solution handles up to 10A**
- **Advantages compared to integrated solutions**
  - **High accuracy (1.5%) fixed voltages; 2.8, 3, 3.3, or 5V**
  - **User flexibility (selection of FET for performance)**
  - **Small footprint with anyCAP™ controller and SMD FET**
  - **Kelvin output sensing possible**
  - **Integral, low-loss current limit sensing for protection**

Figure 7.48: *anyCAP® ADP3310 LDO Regulator Controller Features*

Regulator Controller Differences

An obvious basic difference of the regulator controller versus a stand alone regulator is the removal of the pass device from the regulator chip. This design step has both advantages and disadvantages. A positive is that the external PMOS pass device can be chosen for the exact size, package, current rating and power handling which is most useful to the application. This approach allows the same basic controller IC to be useful for currents of several hundred mA to more than 10 A, simply by choice of the FET. Also, since the regulator controller IC's I_{ground} of 800 µA results is very little power dissipation, its thermal drift will be enhanced. On the downside, there are two packages now used to make up the regulator function. And, current limiting (which can be made completely integral to a standalone IC LDO regulator) is now a function which must be split between the regulator controller IC and an external sense resistor. This step also increases the dropout voltage of the LDO regulator controller somewhat, by about 50 mV.

A functional diagram of the ADP3310 regulator controller is shown in Figure 7.49. The basic error amplifier, reference and scaling divider of this circuit are similar to the standalone anyCAP regulator, and will not be described in detail. The regulator controller version does share the same cap load immunity of the standalone versions, and also has a shutdown function, similarly controlled by the EN (enable) pin.

The main differences in the regulator controller IC architecture is the buffered output of the amplifier, which is brought out on the GATE pin, to drive the external PMOS FET. In addition, the current limit sense amplifier has a built in 50-mV threshold voltage, and is designed to compare the voltage between the V_{IN} and IS pins. When this voltage exceeds 50 mV, the current limit sense amplifier takes over control of the loop, by shutting down the error amplifier and limiting output current to the preset level.

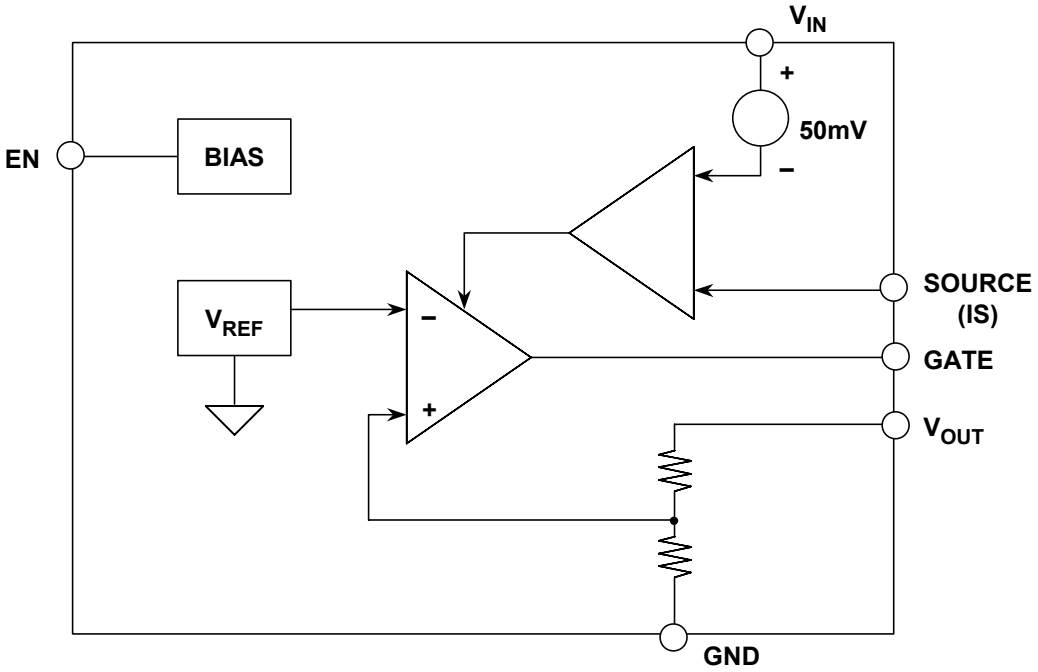


Figure 7.49: *Functional Block Diagram of anyCAP Series LDO Regulator Controller*

A Basic 5-V/1-A LDO Regulator Controller

An LDO regulator controller is easy to use, since a PMOS FET, a resistor and two relatively small capacitors (one at the input, one at the output) is all that is needed to form an LDO regulator. The general configuration is shown by Figure 7.50, an LDO suitable as a 5-V/1-A regulator operating from a V_{IN} of 6 V, using the ADP3310-5 controller IC.

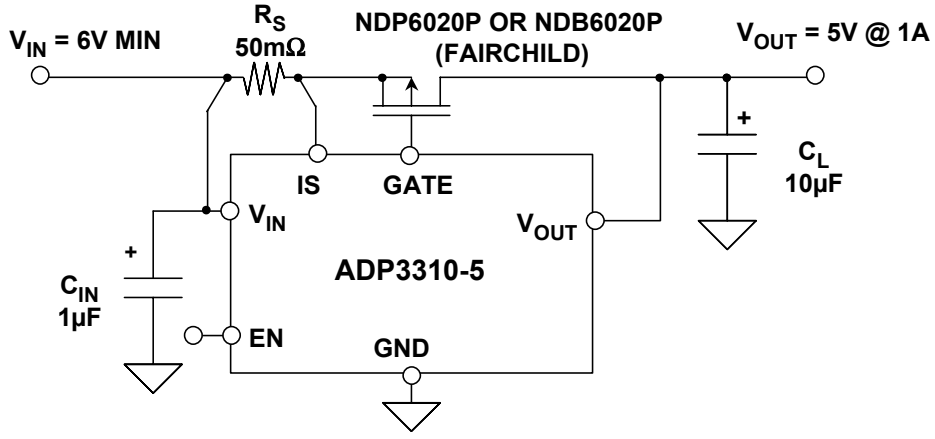


Figure 7.50: *A Basic ADP3310 PMOS FET 1-A LDO Regulator Controller Circuit*

This regulator is stable with virtually any good quality output capacitor used for C_L (as is true with the other anyCAP devices). The actual C_L value required and its associated ESR depends on the g_m and capacitance of the external PMOS device. In general, a 10-µF capacitor at the output is sufficient to ensure stability for load currents up to 10 A. Larger capacitors can also be used, if high output surge currents are present. In such cases, low ESR capacitors such as OS-CON electrolytics are preferred, because they offer lowest ripple on the output. For less demanding requirements, a standard tantalum or aluminum electrolytic can be adequate. When an aluminum electrolytic is used, it should be qualified for adequate performance over temperature. The input capacitor, C_{IN}, is only necessary when the regulator is several inches or more distant from the raw dc filter capacitor. However, since it is a small type, it is usually prudent to use it in most instances, located close to the V_{IN} pin of the regulator.

Selecting the Pass Device

The type and size of the pass transistor are determined by a set of requirements for threshold voltage, input-output voltage differential, load current, power dissipation, and thermal resistance. An actual PMOS pass device selected must satisfy all of these electrical requirements, plus physical and thermal parameters. There are a number of manufacturers offering suitable devices in packages ranging from SO-8 up through TO-220 in size.

To ensure that the maximum available drive from the controller will adequately drive the FET under worst case conditions of temperature range and manufacturing tolerances, the maximum drive from the controller, $V_{GS(DRIVE)}$, to the pass device must be determined. This voltage is calculated as follows:

$$V_{GS(DRIVE)} = V_{IN} - V_{BE} - \left(I_{L(MAX)}\right)\left(R_S\right), \qquad \text{Eq. 7.22}$$

where V_{IN} is the minimum input voltage, $I_{L(MAX)}$ is the maximum load current, R_S the sense resistor, and V_{BE} is a voltage internal to the ADP3310 (~ 0.5 V @ high temp, 0.9 V cold, and 0.7 V at room temp). Note that since $I_{L(MAX)} \times R_S$ will be no more than 75 mV, and V_{BE} at cold temperature ≅0.9 V, this equation can be further simplified to:

$$V_{GS(DRIVE)} \cong V_{IN} - 1\,V\,. \qquad \text{Eq. 7.23}$$

In the Figure 7.50 example, V_{IN} = 6 V and V_{OUT} = 5 V, so $V_{GS(DRIVE)}$ is 6 – 1 = 5 V.

It should be noted that the above two equations apply to FET drive voltages which are *less* than the typical gate-to-source clamp voltage of 8 V (built into the ADP3310, for the purposes of FET protection).

An overall goal of the design is to then select an FET which will have an $R_{DS(ON)}$ sufficiently low so that the resulting dropout voltage will be less than $V_{IN} - V_{OUT}$, which in this case is 1 V. For the NDP6020P used in Fig. 7.50 (see Reference 10), this device achieves an $R_{DS(ON)}$ of 70-milliohms (max) with a V_{GS} of 2.7 V, a voltage drive appreciably less than the ADP3310's $V_{GS(DRIVE)}$ of 5V. The dropout voltage V_{MIN} of this

regulator configuration is the sum of two series voltage drops, the FET's drop plus the drop across R_S, or:

$$V_{MIN} = I_{L(MAX)}\left(R_{DS(ON)} + R_S\right). \quad \text{Eq. 7.24}$$

In the design here, the two resistances are roughly comparable to one another, so the net V_{MIN} will be 1 A × (50 + 70 milliohms) = 120 mV.

For a design safety margin, use a FET with a rated V_{GS} at the required $R_{DS,}$ with a substantial headroom between the applicable ADP3310 $V_{GS(DRIVE)}$ and the applicable V_{GS} rating for the FET. In the case here, there is ample margin, with 5 V of drive and a V_{GS} of 2.7 V. It should be borne in mind that the FET's V_{GS} and $R_{DS(ON)}$ will change over temperature, but for the NDP6020P device even these variations and a V_{GS} of 4.5 V are still possible with the circuit as shown. With a rated minimum dc input of 6 V, this means that the design is conservative with 5-V output. In practice, the circuit will typically operate with input voltage minimums on the order of V_{OUT} plus the dropout of 120 mV, or ~ 5.12 V. Since the NDP6020P is also a fairly low threshold device, it will typically operate at lower output voltages, down to about 3 V.

In the event the output is shorted to ground, the pass device chosen must be able to conduct the maximum short circuit current, both instantaneously and longer term.

Thermal Design

The maximum allowable thermal resistance between the FET junction and the highest expected ambient temperature must be taken into account, to determine the type of FET package and heat sink used (if any).

Whenever possible to do so reliably, the FET pass device can be directly mounted to the PCB, and the available PCB copper lands used as an effective heat sink. This heat sink philosophy will likely be adequate when the power to be dissipated in the FET is on the order of 1-2 W or less. Note that the very nature of an LDO helps this type of design immensely, as the lower voltage drop across the pass device reduces the power to be dissipated. Under normal conditions for example, Q1 of Figure 7.52 dissipates less than 1 W at a current of 1 A, since the drop across the FET is less than 1 V.

To use PCB lands as effective heat sinks with SO-8 and other SMD packages, the pass device manufacturer's recommendations for the lowest θ_{JA} mounting should be followed (see References 11 and 12). In general these suggestions will likely parallel the 5 rules noted above, under "LDO regulator thermal considerations" for SO-8 and SOT-23 packaged anyCAP LDOs. For lowest possible thermal resistance, also connect multiple FET pins together, as follows:

Electrically connect multiple FET source and drain pins in parallel, as well as to the corresponding R_S and V_{OUT} large area PCB lands.

Using 2-oz. copper PCB material and one square inch of copper PCB land area as a heatsink, it is possible to achieve a net thermal resistance, θ_{JA}, for mounted SO-8 devices

on the order of 60°C/W or less. Such data is available for SO-8 power FETs (see Reference 11). There are also a variety of larger packages with lower thermal resistance than the SO-8, but still useful with surface mount techniques. Examples are the DPAK and D^2PAK, etc.

For higher power dissipation applications, corresponding to thermal resistance of 50°C/W or less, a bolt-on external heat sink is required to satisfy the θ_{JA} requirement. Compatible package examples would be the TO-220 family, which is used with the NDP6020P example of Fig. 7.52.

Calculating thermal resistance for $V_{IN} = 6.7$ V, $V_{OUT} = 5$ V, and $I_L = 1$ A:

$$\theta_{JA} = \frac{T_J - T_{A(MAX)}}{V_{DS(MAX)} \cdot I_L}, \qquad \text{Eq. 7.25}$$

where T_J is the pass device junction temperature limit, $T_{A(MAX)}$ is the maximum ambient temperature, $V_{DS(MAX)}$ is the maximum pass device drain-source voltage, and $I_{L(MAX)}$ is the maximum load current.

Inserting some example numbers of 125°C as a max. junction temp for the NDP6020P, a 75°C expected ambient, and the $V_{DS(MAX)}$ and $I_{L(MAX)}$ figures of 1.7 V and 1 A, the required θ_{JA} works out to be (125°C – 75°C) /1.7 = 29.4°C/W. This can be met with a very simple heat sink, which is derived as follows.

The NDP6020P in the TO-220 package has a junction-case thermal resistance, θ_{JC}, of 2°C/W. The required external heatsink's thermal resistance, θ_{CA}, is determined as follows:

$$\theta_{CA} = \theta_{JA} - \theta_{JC}, \qquad \text{Eq. 7.26}$$

where θ_{CA} is the required heat sink case-to-ambient thermal resistance, θ_{JA} is the calculated *overall* junction-to-ambient thermal resistance, and θ_{JC} is the pass device junction-to-case thermal resistance, which in this case is 2°C/W typical for TO-220 devices, and NDP6020P.

$$\theta_{CA} = 29.4°C/W - 2°C/W = 27.4°C/W. \qquad \text{Eq. 7.27}$$

For a safety margin, select a heatsink with a θ_{CA} *less* than the results of this calculation. For example, the Aavid TO-220 style clip on heat sink # 576802 has a θ_{CA} of 18.8°C/W, and in fact many others have performance of 25°C/W or less. As an alternative, the NDB6020P D^2PAK FET pass device could be used in this same design, with an SMD style heat sink such as the Aavid 573300 series used in conjunction with an internal PCB heat spreader.

Note that many LDO applications like the above will calculate out with very modest heat sink requirements. This is fine, as long as the output never gets shorted! With a shorted output, the current goes to the limit level (as much as 1.5 A in this case), while the

voltage across the pass device goes to V_{IN} (which could also be at a maximum). In this case, the new pass device dissipation for short circuit conditions becomes 1.5 A × 6.7 V, or 10 W. Supporting this level of power continuously will require the entire heat sink situation to be re-evaluated, as what was adequate for 1.7 W will simply not be adequate for 10 W. In fact, the required heat sink θ_{CA} is about 3°C/W to support the 10 W safely on a continuous basis, which requires a much larger heat sink.

Sensing Resistors for LDO Controllers

Current limiting in the ADP3310 controller is achieved by choosing an appropriate external current sense resistor, R_S, which is connected between the controller's V_{IN} and IS (source) pins. An internally derived 50-mV current limit threshold voltage appears between these pins, to establish a comparison threshold for current limiting. This 50 mV determines the threshold where current limiting begins. For a continuous current limiting, a foldback mode is established, with dissipation controlled by reducing the gate drive. The net effect is that the ultimate current limit level is a factor of 2/3 of maximum. The foldback limiting reduces the power dissipated in the pass transistor substantially.

To choose a sense resistor for a maximum output current I_L, R_S is calculated as follows:

$$R_S = \frac{0.05}{K_F \cdot I_L}. \qquad \text{Eq. 7.28}$$

In this expression, the nominal 50-mV current limit threshold voltage appears in the numerator. In the denominator appears a scaling factor K_F, which can be either 1.0 or 1.5, plus the maximum load current, I_L. For example, if a scaling factor of 1.0 is to be used for a 1-A I_L, the R_S calculation is straightforward, and 50 milliohms is the correct R_S value.

However, to account for uncertainties in the threshold voltage and to provide a more conservative output current margin, a scaling factor of $K_F = 1.5$ can alternately be used. When this approach is used, the same 1-A I_L load conditions will result in a 33-milliohm R_S value. In essence, the use of the 1.5 scaling factor takes into account the foldback scheme's reduction in output current, allowing higher current in the limit mode.

The simplest and least expensive sense resistor for high current applications such as Figure 7.50 is a copper PCB trace controlled in both thickness and width. Both the temperature dependence of copper and the relative size of the trace must be taken into account in the resistor design. The temperature coefficient of resistivity for copper has a positive temperature coefficient of +0.39%/°C. This natural copper TC, in conjunction with the controller's PTAT based current limit threshold voltage, can provide for a current limit characteristic which is simple and effective over temperature.

The table of Figure 7.51 provides resistance data for designing PCB copper traces with various PCB copper thickness (or weight), in ounces of copper per square foot area. To use this information, note that the center column contains a resistance coefficient, which is the conductor resistance in milliohms/inch, divided by the trace width, W. For example, the first entry, for 1/2 ounce copper is 0.983 milliohms/inch/W. So, for a reference trace width of 0.1", the resistance would be 9.83 milliohms/inch. Since these

are all linear relationships, everything scales for wider/skinnier traces, or for differing copper weights. As an example, to design a 50 milliohm R_S for the circuit of Fig. 7.50 using 1/2 ounce copper, a 2.54" length of a 0.05" wide PCB trace could be used.

Copper Thickness	Resistance Coefficient, milliohms / inch/ W (trace width W in inches)	Reference 0.1 inch wide trace, milliohms / inch
1/2 oz / ft^2	0.983 / W	9.83
1 oz / ft^2	0.491 / W	4.91
2 oz / ft^2	0.246 / W	2.46
3 oz / ft^2	0.163 / W	1.63

Figure 7.51: *Printed Circuit Copper Resistance Design for LDO Controllers*

To minimize current limit sense voltage errors, the two connections to R_S should be made four-terminal style, as is noted in Figure 7.50 (again). It is not absolutely necessary to actually use four-terminal style resistors, except for the highest current levels. However, as a minimum, the heavy currents flowing in the source circuit of the pass device should not be allowed to flow in the ADP3310 sense pin traces. To minimize such errors, the V_{IN} connection trace to the ADP3310 should connect close to the body of R_S (or the resistor's input sense terminal), and the IS connection trace should also connect close to the resistor body (or the resistor's output sense terminal). Four-terminal wiring is increasingly important for output currents of 1 A or more.

Alternately, an appropriate selected sense resistor such as surface mount sense devices available from resistor vendors can be used (see Reference 13). Sense resistor R_S may not be needed in all applications, if a current limiting function is provided by the circuit feeding the regulator. For circuits that don't require current limiting, the IS and V_{IN} pins of the ADP3310 must be tied together.

PCB-Layout Issues

For best voltage regulation, place the load as close as possible to the controller device's V_{OUT} and GND pins. Where the best regulation is required, the V_{OUT} trace from the ADP3310 and the pass device's drain connection should connect to the positive load terminal via separate traces. This step (Kelvin sensing) will keep the heavy load currents in the pass device's drain out of the feedback sensing path, and thus maximize output accuracy. Similarly, the unregulated input common should connect to the common side of the load via a separate trace from the ADP3310 GND pin.

A 2.8-V / 8-A LDO Regulator Controller

With seemingly minor changes to the basic 1-A LDO circuit used in Fig. 7.50, an 8-A LDO regulator controller can be configured, as shown in Figure 7.52. This circuit uses an ADP3310-2.8, to produce a 2.8-V output. The sense resistor is dropped to 5 milliohms, which supports currents of up to 10 A (or about 6.7 A, with current limiting active). Four-terminal wiring should be used with the sense resistor to minimize errors.

The most significant change over the more generic schematic of Fig. 7.50 is the use of multiple, low ESR input and output bypass capacitors. At the output, C2 is a bank of 4 × 220-µF OS-CON type capacitors, in parallel with 2 × 10-µF MLCC chip type capacitors. These are located right at the load point with minimum inductance wiring, plus separate wiring back to the V_{OUT} pin of the ADP3310 and the drain of the pass device. This wiring will maximize the dc output accuracy, while the multiple capacitors will minimize the transient errors at the point-of-load. In addition, multiple bypasses on the regulator input in the form of C1 minimizes the transient errors at the regulator's V_{IN} pin.

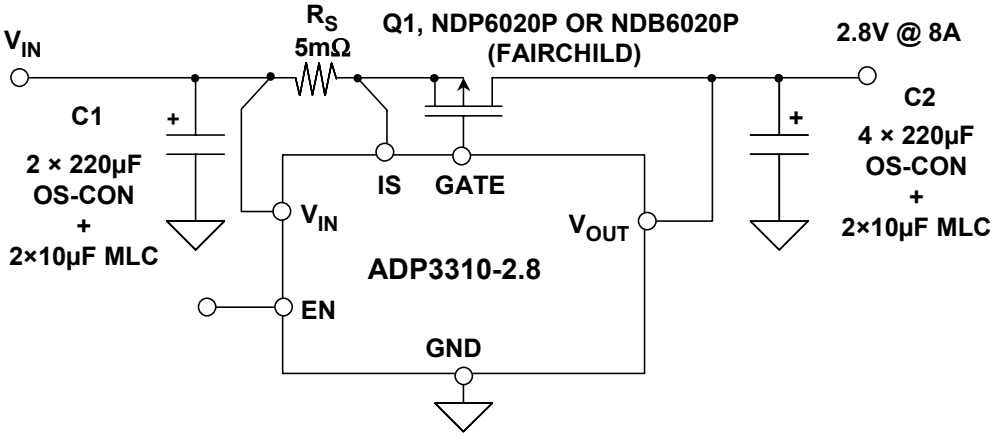


Figure 7.52: *A 2.8 V/8 A LDO Regulator Controller*

Heat sink requirements for the pass device in this application will be governed by the loading and input voltage, and should be calculated by the procedures discussed above.

REFERENCES:
7.2 LOW DROPOUT LINEAR REGULATORS

1. Bob Widlar, "New Developments in IC Voltage Regulators," **IEEE Journal of Solid State Circuits**, Vol. SC-6, February, 1971.

2. Robert C. Dobkin, "3-Terminal Regulator is Adjustable," **National Semiconductor AN-181**, March, 1977.

3. Paul Brokaw, "A Simple Three-Terminal IC Bandgap Voltage Reference," **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

4. Frank Goodenough, "Linear Regulator Cuts Dropout Voltage," **Electronic Design**, April 16, 1987.

5. Chester Simpson, "LDO Regulators Require Proper Compensation," **Electronic Design**, November 4, 1996.

6. Frank Goodenough, "Vertical-PNP-Based Monolithic LDO Regulator Sports Advanced Features," **Electronic Design**, May 13, 1996.

7. Frank Goodenough, "Low Dropout Regulators Get Application Specific," **Electronic Design**, May 13, 1996.

8. Jim Solomon, "The Monolithic Op Amp: A Tutorial Study." **IEEE Journal of Solid State Circuits**, Vol. SC-9, No.6, December 1974.

9. Richard J. Reay, Gregory T.A. Kovacs, "An Unconditionally Stable Two-Stage CMOS Amplifier," **IEEE Journal of Solid State Circuits**, Vol. SC-30, No.5, May 1995.

10. NDP6020P / NDB6020P P-Channel Logic Level Enhancement Mode Field Effect Transistor, Fairchild Semiconductor data sheet, September 1997, http://www.fairchildsemi.com.

11. Alan Li, et all, "Maximum Power Enhancement Techniques for SO-8 Power MOSFETs," **Fairchild Semiconductor application note AN1029**, April 1996, http://www.fairchildsemi.com.

12. Rob Blattner, Wharton McDaniel, "Thermal Management in On-Board DC-to-DC Power Conversion," **Temic application note**, http://www.temic.com.

13. "S" series surface mount current sensing resistors, KRL/Bantry Components, 160 Bouchard Street, Manchester, NH, 03103-3399, (603) 668-3210.

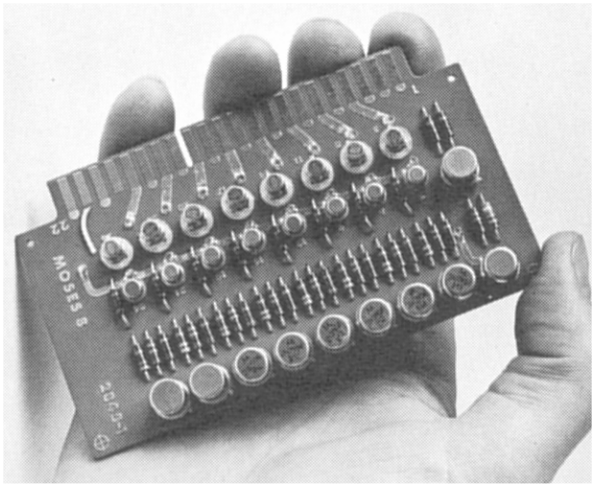
SECTION 7.3: ANALOG SWITCHES AND MULTIPLEXERS

Walt Kester

Introduction

Solid-state analog switches and multiplexers have become an essential component in the design of electronic systems which require the ability to control and select a specified transmission path for an analog signal. These devices are used in a wide variety of applications including multi-channel data acquisition systems, process control, instrumentation, video systems, etc.

One of the first commercial analog multiplexers is shown in Figure 7.53, the MOSES-8 from the Pastoriza Division of Analog Devices in 1969. This PC board multiplexer consisted of 8 MOSFET switches and 8 switch drivers. The part had a switching time of 100 ns, on-resistance of 500 Ω. Selling price in 1969 was $320. For ±5-V inputs, the multiplexer operated on ±15-V supplies, but for ±10-V inputs, it required not only the +15 V but also a –28-V supply. Today, the ADG725/ADG726/ADG731/ADG732 family offers a 32-channel multiplexer with 4-Ω on-resistance, 20-µA quiescent current, and packaged in 7 mm × 7 mm chip scale (CSP) or thin plastic quad flatpack (TQFP). The price is less than $5.



- 8 Channels
- Switching time: 100 ns
- On Resistance: 500Ω
- Off Resistance: > 100MΩ
- $320

TODAY:

ADG725,ADG726, ADG731, ADG732:

- 32 Channels
- Switching Time: 30ns
- On Resistance: 4Ω
- 7 mm^2 CSP or TQFP
- < $5

Figure 7.53: *"MOSES-8" MOSFET Analog Multiplexer Analog Devices' Pastoriza Division, 1969*

With the development of CMOS processes (yielding good PMOS and NMOS transistors on the same substrate), switches and multiplexers rapidly gravitated to integrated circuit form in the mid-1970s, with product introductions such as the Analog Devices' popular AD7500-series (introduced in 1973). A dielectrically-isolated family of these parts introduced in 1976 allowed input overvoltages of ±25 V (beyond the supply rails) and was insensitive to latch-up.

These early CMOS switches and multiplexers were typically designed to handle signal levels up to ±10 V while operating on ±15-V supplies. In 1979, Analog Devices introduced the popular ADG200-series of switches and multiplexers, and in 1988 the ADG201-series was introduced which was fabricated on a proprietary linear-compatible CMOS process (LC^2MOS). These devices allowed input signals to ±15 V when operating on ±15-V supplies.

A large number of switches and multiplexers were introduced in the 1980s and 1990s, with the trend toward lower on-resistance, faster switching, lower supply voltages, lower cost, lower power, and smaller surface-mount packages.

Today, analog switches and multiplexers are available in a wide variety of configurations, options, etc., to suit nearly all applications. On-resistances less than 0.5 Ω, picoampere leakage currents, signal bandwidths greater than 1 GHz, and single 1.8-V supply operation are now possible with modern CMOS technology.

Although CMOS is by far the most popular IC process today for switches and multiplexers, bipolar processes (with JFETs) and complementary bipolar processes (also with JFET capability) are often used for special applications such as video switching and multiplexing where the high performance characteristics required are not attainable with CMOS. Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time is generally not fast enough, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch on-resistance with signal level (R_{ON} modulation) can introduce unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer better solutions at video frequencies—with obvious power and cost increases above CMOS devices.

CMOS Switch Basics

The ideal analog switch has no on-resistance, infinite off-impedance and zero time delay, and can handle large signal and common-mode voltages. Real CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the "on" state, its resistance can be less than 1 Ω, while in the "off" state, the resistance increases to several hundreds of megohms, with picoampere leakage currents. CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease. A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 7.54.

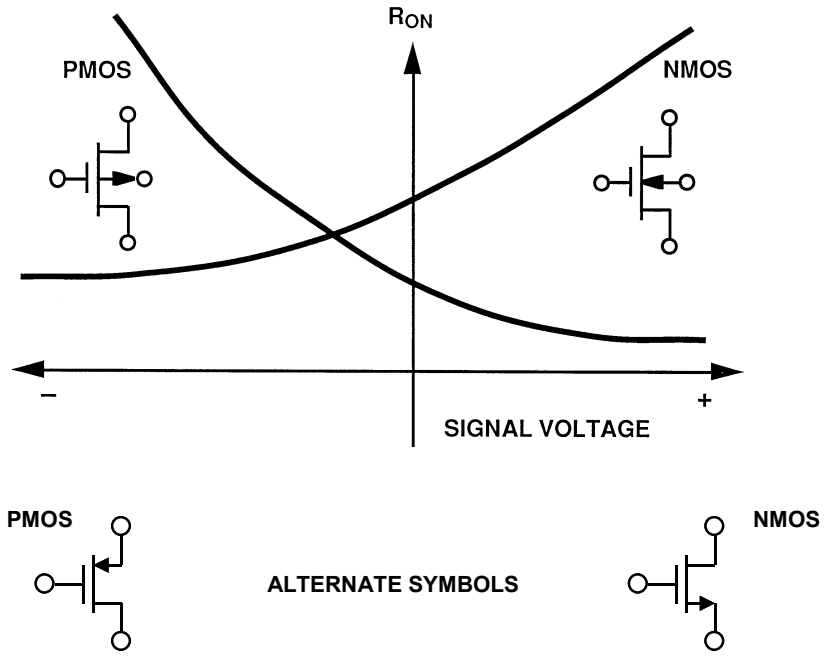


Figure 7.54: *MOSFET Switch ON-Resistance Versus Signal Voltage*

The complementary-MOS process (CMOS) yields good P-channel and N-channel MOSFETs. Connecting the PMOS and NMOS devices in parallel forms the basic bilateral CMOS switch of Figure 7.55. This combination reduces the on-resistance, and also produces a resistance which varies much less with signal voltage.

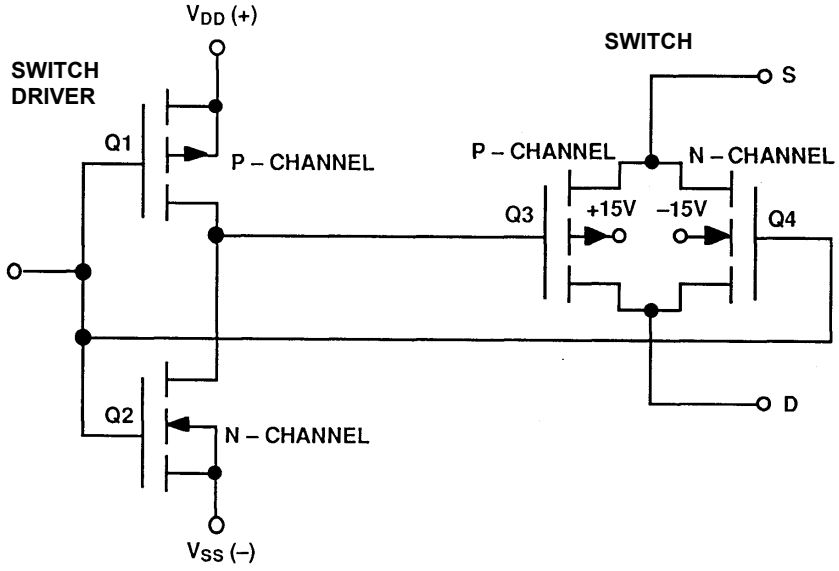


Figure 7.55: *Basic CMOS Switch Uses Complementary Pair to Minimize R_{ON} Variation due to Signal Swings*

Figure 7.56 shows the on-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can causes errors in dc accuracy as well as ac distortion. The bilateral CMOS switch solves this problem. On-resistance is minimized, and linearity is also improved. The bottom curve of Figure 7.56 shows the improved flatness of the on-resistance characteristic of the switch.

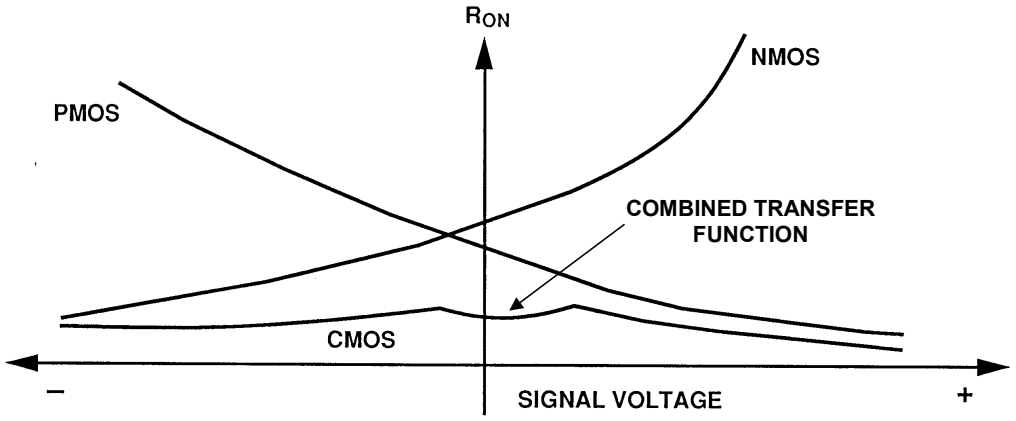


Figure 7.56: *CMOS Switch ON-Resistance Versus Signal Voltage*

The ADG8xx-series of CMOS switches are specifically designed for less than 0.5-Ω on-resistance and are fabricated on a sub-micron process. These devices can carry currents up to 400 mA, operate on a single 1.8-V to 5.5-V supply, and are rated over an extended temperature range of –40°C to +125°C. On-resistance over temperature and input signal level is shown in Figure 7.57.

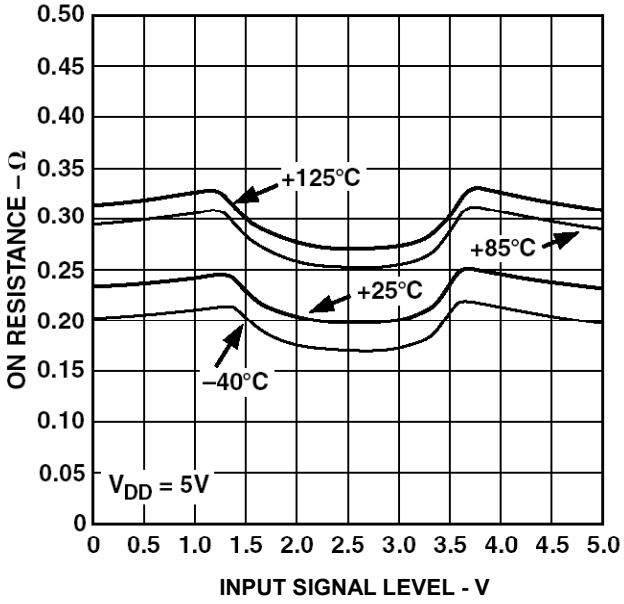


Figure 7.57: *ON-Resistance Versus Input Signal for ADG801/ADG802 CMOS Switch, V_{DD} = +5 V*

Error Sources in the CMOS Switch

It is important to understand the error sources in an analog switch. Many affect ac and dc performance, while others only affect ac. Figure 7.58 shows the equivalent circuit of two adjacent CMOS switches. The model includes leakage currents and junction capacitances.

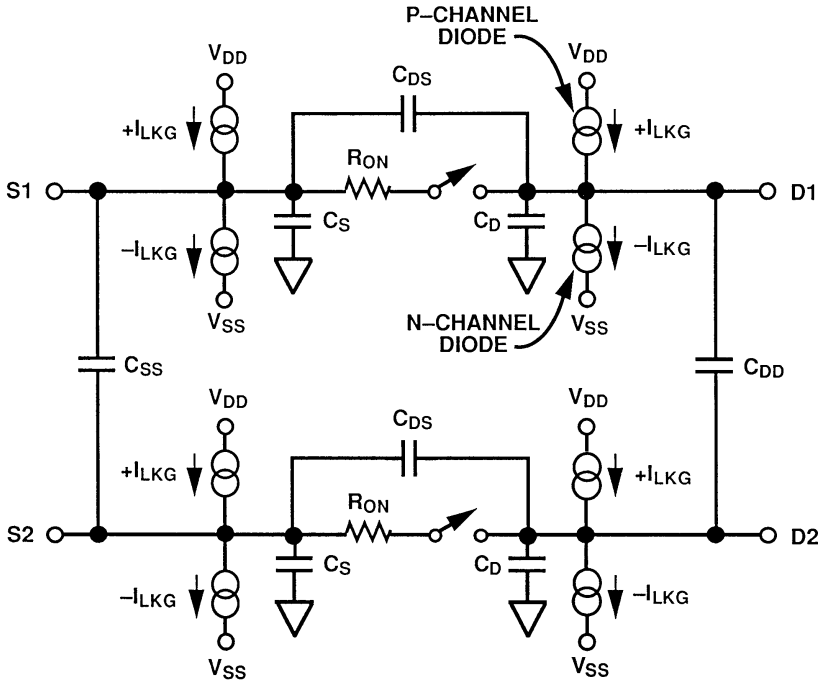
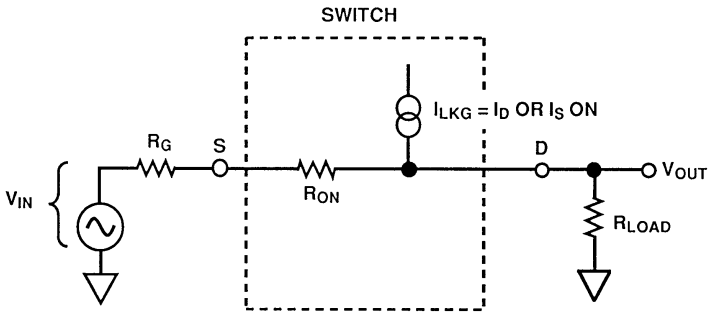


Figure 7.58: *Equivalent Circuit of Two Adjacent CMOS Switches*

dc errors associated with a single CMOS switch in the on state are shown in Figure 7.59. When the switch is on, dc performance is affected mainly by the switch on-resistance (R_{ON}) and leakage current (I_{LKG}). A resistive attenuator is created by the R_G-R_{ON}-R_{LOAD} combination which produces a gain error. The leakage current, I_{LKG}, flows through the equivalent resistance of R_{LOAD} in parallel with the sum of R_G and R_{ON}. Not only can R_{ON} cause gain errors—which can be calibrated using a system gain trim—but its variation with applied signal voltage (R_{ON} modulation) can introduce distortion—for which there is no calibration. Low resistance circuits are more subject to errors due to R_{ON}, while high resistance circuits are affected by leakage currents. Figure 7.59 also gives equations that show how these parameters affect dc performance.

When the switch is OFF, leakage current can introduce errors as shown in Figure 7.60. The leakage current flowing through the load resistance develops a corresponding voltage error at the output.

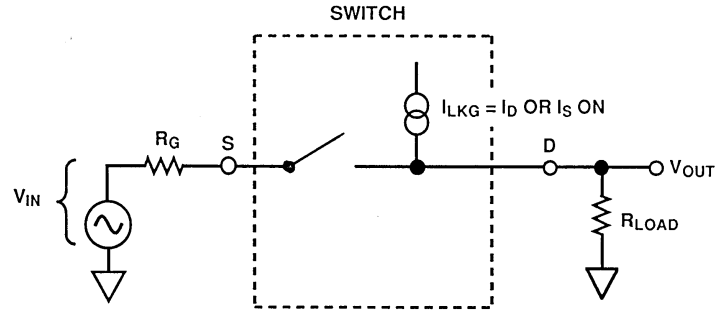


$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

IF $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}}\right]$$

Figure 7.59: *Factors Affecting DC Performance for ON Switch Condition: R_{ON}, R_{LOAD}, and I_{LKG}*

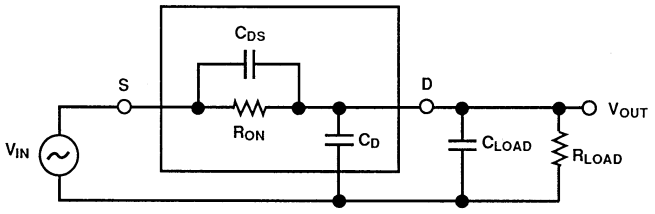


Leakage current creates error voltage at V_{OUT} equal to:

$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 7.60: *Factors Affecting DC Performance for OFF Switch Condition: I_{LKG} and R_{LOAD}*

Figure 7.61 illustrates the parasitic components that affect the ac performance of CMOS switches. Additional external capacitances will further degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth. C_{DS} (drain-to-source capacitance), C_D (drain-to-ground capacitance), and C_{LOAD} all work in conjunction with R_{ON} and R_{LOAD} to form the overall transfer function.



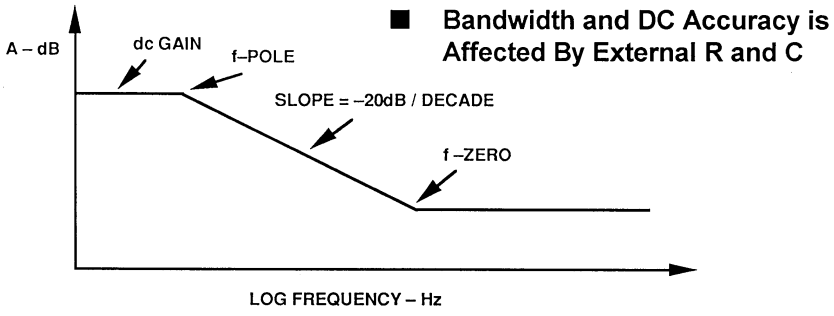
$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right]\left[\frac{sR_{ON}C_{DS} + 1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

$$A(dB) = 20\log\left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right] + 10\log\left[\omega^2(R_{ON}C_{DS})^2 + 1\right] - 10\log\omega^2\left[\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)^2(C_{LOAD} + C_D + C_{DS})^2 + 1\right]$$

Figure 7.61: *Dynamic Performance Considerations: Transfer Accuracy Versus Frequency*

In the equivalent circuit, C_{DS} creates a frequency zero in the numerator of the transfer function A(s). This zero usually occurs at high frequencies because the switch on-resistance is small. The bandwidth is also a function of the switch output capacitance in combination with C_{DS} and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 7.62 which shows the overall Bode plot for the switch in the on state. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance C_D. Thus, to maximize bandwidth, a switch should have low input and output capacitance and low on-resistance.

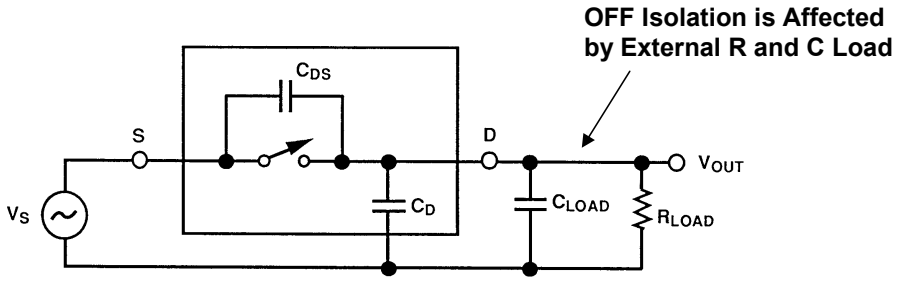


$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right][sR_{ON}C_{DS} + 1]\left[\frac{1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

$$DC\ GAIN = \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}},\quad f_{ZERO} = \frac{0.159}{R_{ON}C_{DS}},\quad f_{POLE} = \frac{0.159}{\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS})}$$

Figure 7.62: *Bode Plot of CMOS Switch Transfer Function in the ON State*

The series-pass capacitance, C_{DS}, not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch during its OFF state. When the switch is off, C_{DS} couples the input signal to the output load as shown in Figure 7.63.



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 7.63: *Dynamic Performance Considerations: Off Isolation*

Large values of C_{DS} will produce large values of feedthrough, proportional to the input frequency. Figure 7.64 illustrates the drop in OFF-isolation as a function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a C_{DS} as possible.

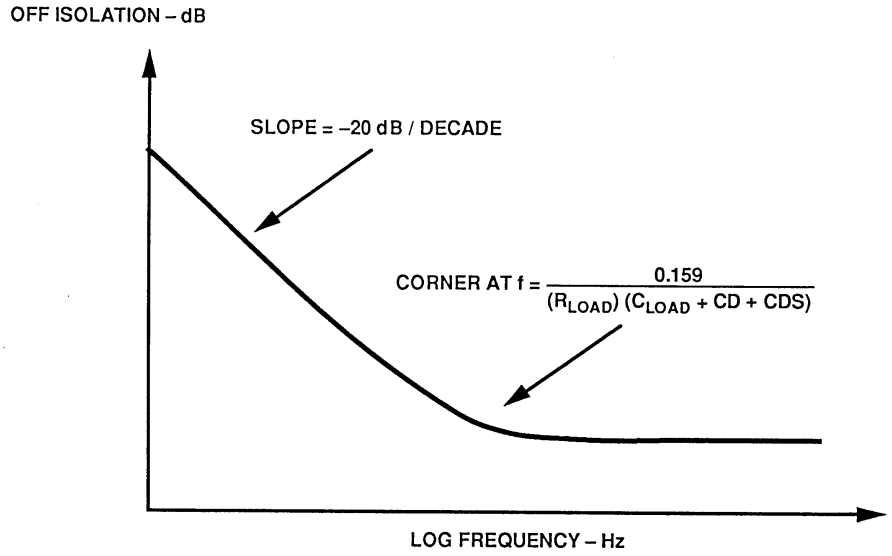


Figure 7.64: *Off Isolation Versus Frequency*

Figure 7.65 shows typical CMOS analog switch OFF-isolation as a function of frequency for the ADG708 8-channel multiplexer. From dc to several kilohertz, the multiplexer has nearly 90-dB isolation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 10 MHz, the switch shown still has nearly 60-dB of isolation.

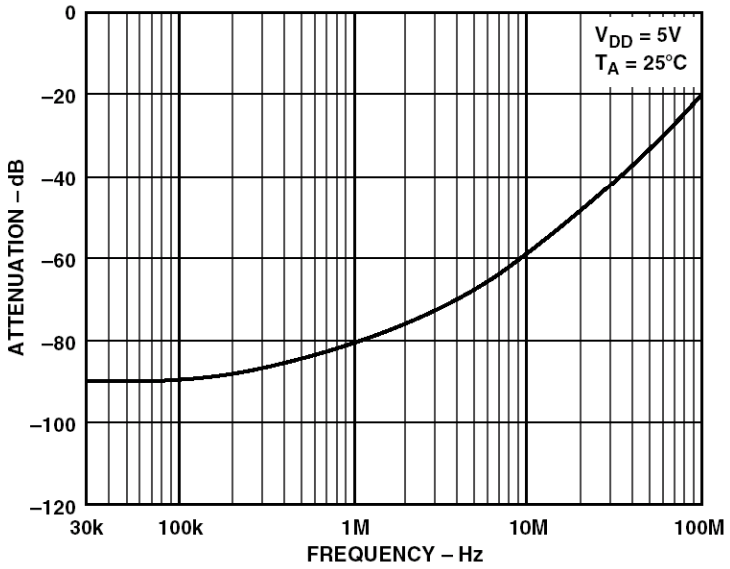


Figure 7.65: *OFF-Isolation Versus Frequency for ADG708 8-Channel Multiplexer*

Another ac parameter that affects system performance is the charge injection that takes place during switching. Figure 7.66 shows the equivalent circuit of the charge injection mechanism.

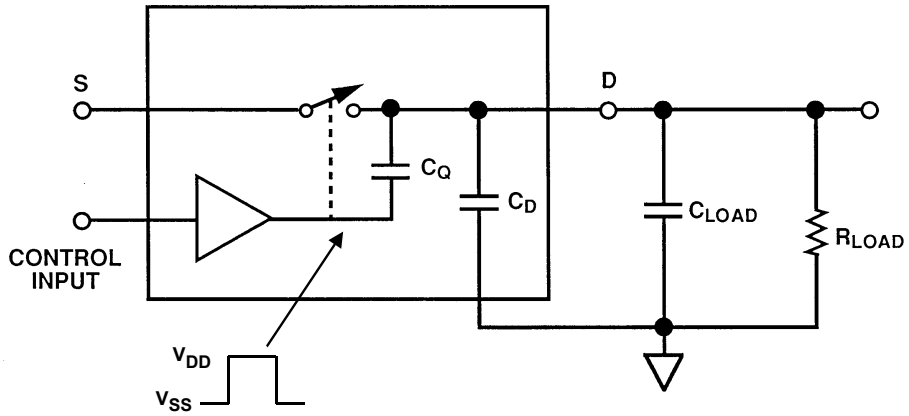


Figure 7.66: *Dynamic Performance Considerations: Charge Injection Model*

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS}, or vice versa) at the gate of the CMOS switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance C_Q. The amount of charge coupled depends on the magnitude of the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching as shown in Figure 7.67. The change in output voltage, ΔV_{OUT}, is a function of the amount of charge injected, Q_{INJ} (which is in turn a function of the gate-drain capacitance, C_Q) and the load capacitance, C_L.

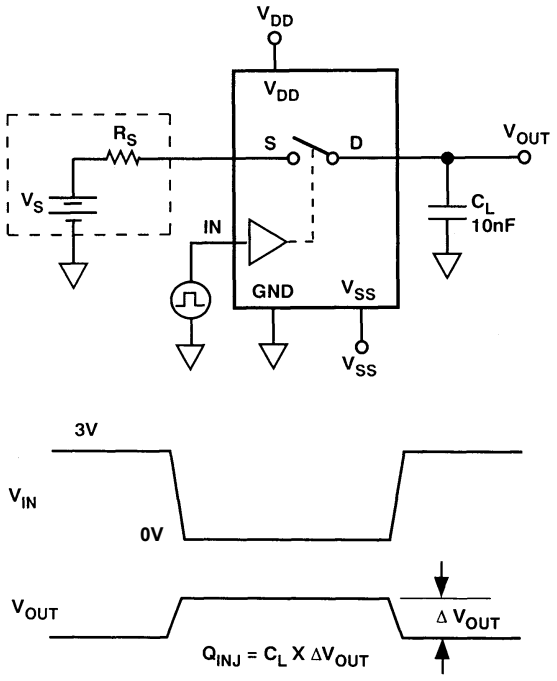


Figure 7.67: *Effects of Charge Injection on Output*

Another problem caused by switch capacitance is the retained charge when switching channels. This charge can cause transients in the switch output, and Figure 7.68 illustrates the phenomenon.

Assume that initially S2 is closed and S1 open. C_{S1} and C_{S2} are charged to –5 V. As S2 opens, the –5 V remains on C_{S1} and C_{S2}, as S1 closes. Thus, the output of Amplifier A sees a –5-V transient. The output will not stabilize until Amplifier A's output fully discharges C_{S1} and C_{S2} and settles to 0 V. The scope photo in Figure 7.69 depicts this transient. The amplifier's transient load settling characteristics will therefore be an important consideration when choosing the right input buffer.

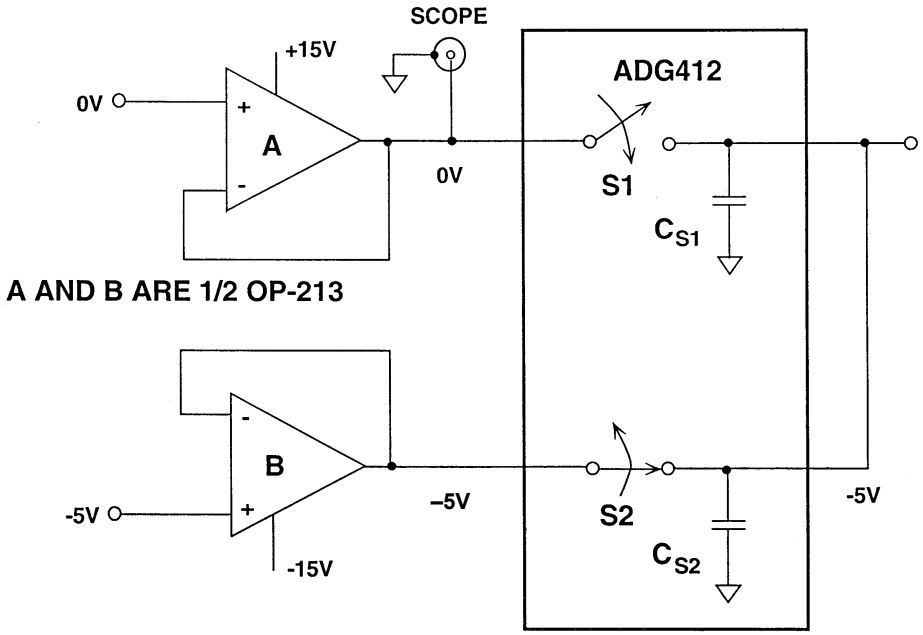


Figure 7.68: *Charge Coupling Causes Dynamic Settling Time Transient When Multiplexing Signals*

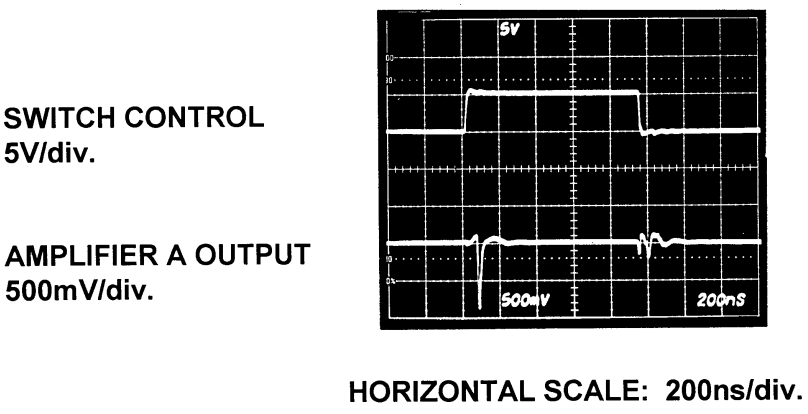


Figure 7.69: *Output of Amplifier Shows Dynamic Settling Time Transient Due to Charge Coupling*

Crosstalk is related to the capacitances between two switches. This is modeled as the C_{SS} capacitance shown in Figure 7.70.

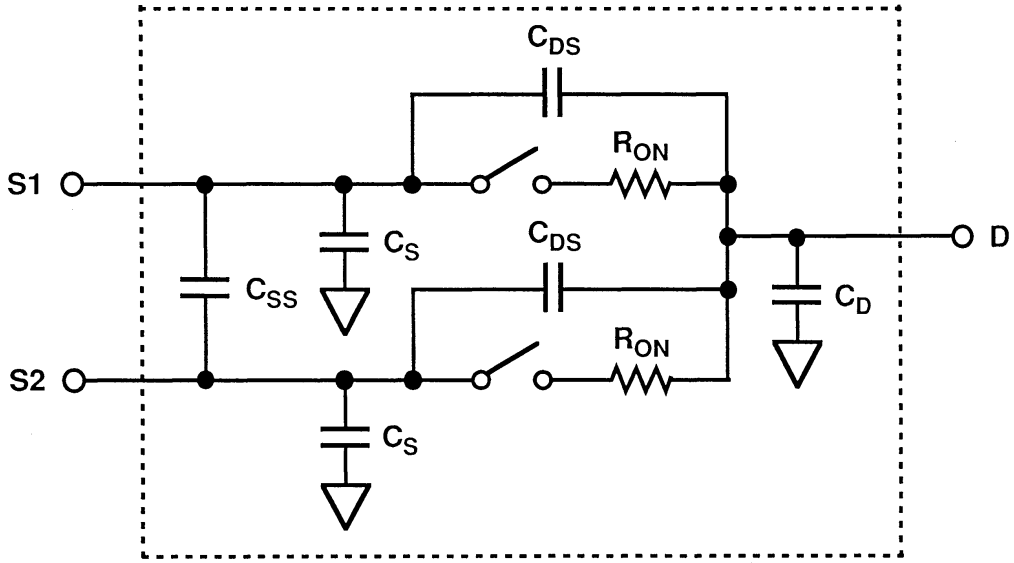


Figure 7.70: *Channel-to-Channel Crosstalk Equivalent Circuit for Adjacent Switches*

Figure 7.71shows typical crosstalk performance of the ADG708 8-channel CMOS multiplexer.

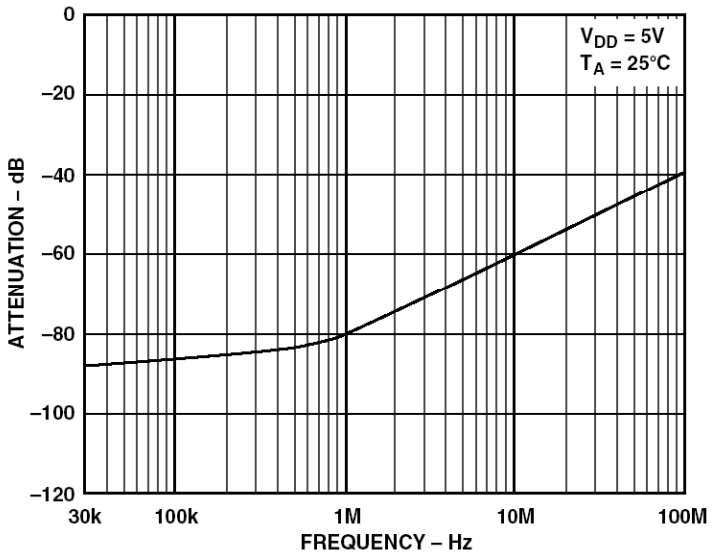
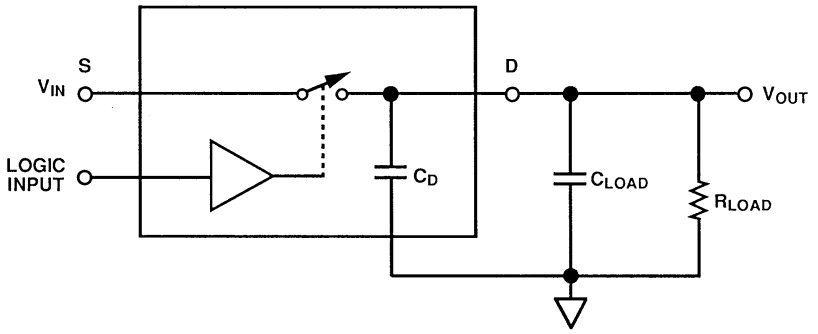


Figure 7.71: *Crosstalk Versus Frequency for ADG708 8-Channel Multiplexer*

Finally, the switch itself has a settling time that must be considered. Figure 7.72 shows the dynamic transfer function. The settling time can be calculated, because the response is a function of the switch and circuit resistances and capacitances. One can assume that this is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy as shown in Figure 7.73.



$$\text{OFF-TO-ON:}\quad t_{SETT} = t_{ON} + \left(\frac{R_{ON}R_{LOAD}}{R_{ON}+R_{LOAD}}\right)(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

$$\text{ON-TO-OFF:}\quad t_{SETT} = t_{OFF} + (R_{LOAD})(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

Settling time is the time required for the switch output to settle within a given error band of the final value.

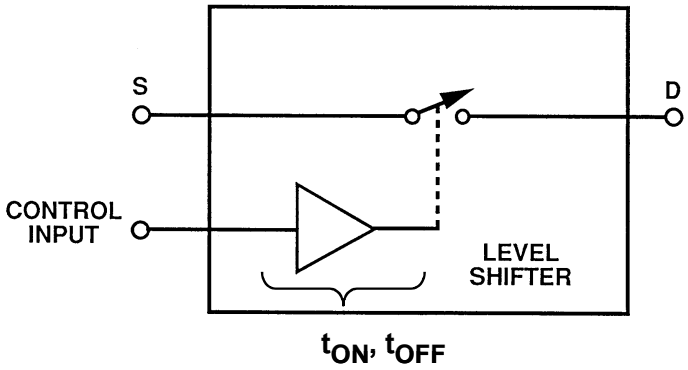
Figure 7.72: *Multiplexer Settling Time*

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS
6	1.563	4.16
8	0.391	5.55
10	0.0977	6.93
12	0.0244	8.32
14	0.0061	9.70
16	0.00153	11.09
18	0.00038	12.48
20	0.000095	13.86
22	0.000024	15.25

Figure 7.73: *Number of Time Constants Required to Settle to 1 LSB Accuracy for a Single-Pole System*

Applying the Analog Switch

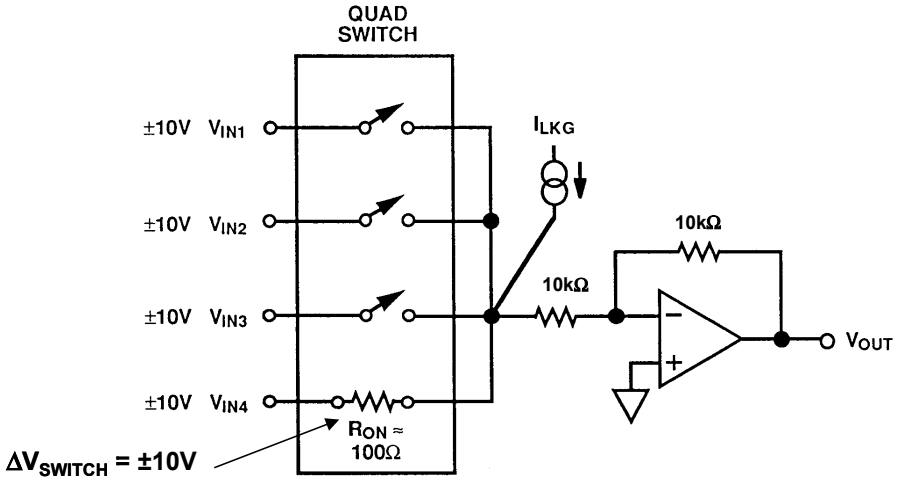
Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propagation delay from the control input to the toggling of the switch, and are largely caused by time delays in the drive and level-shift circuits (see Figure 7.74). The t_{ON} and t_{OFF} values are generally measured from the 50% point of the control input leading edge to the 90% point of the output signal level.



- **t_{ON} and t_{OFF} should not be confused with settling time.**
- **t_{ON} and t_{OFF} are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.**
- **t_{ON} and t_{OFF} are measured from the 50% point of the control input to the 90% point of the output signal level.**

Figure 7.74: *Applying the Analog Switch: Dynamic Performance Considerations*

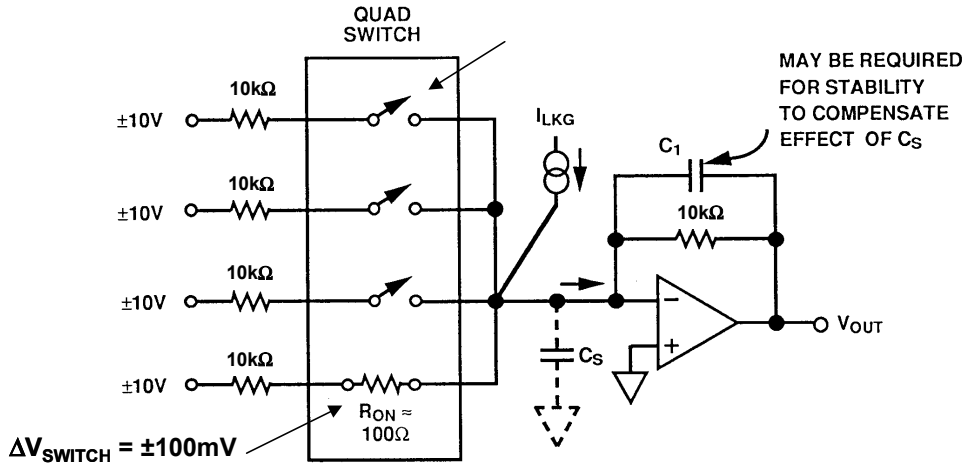
We will next consider the issues involved in buffering a CMOS switch or multiplexer output using an op amp. When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the on-resistance, and its nonlinear change as a function of input voltage, will cause gain and distortion errors as shown in Figure 7.75. If the resistors are large, the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of R_{ON}.



- **ΔR_{ON} caused by ΔV_{IN} , degrades linearity of V_{OUT} relative to V_{IN}.**
- **ΔR_{ON} causes overall gain error in V_{OUT} relative to V_{IN} .**

Figure 7.75: *Applying the Analog Switch: Unity Gain Inverter with Switched Input*

To minimize the effect of R_{ON} change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 7.76. This ensures the switches are only modulated with about ±100 mV rather than the full ±10 V—but a separate resistor is required for each input leg.



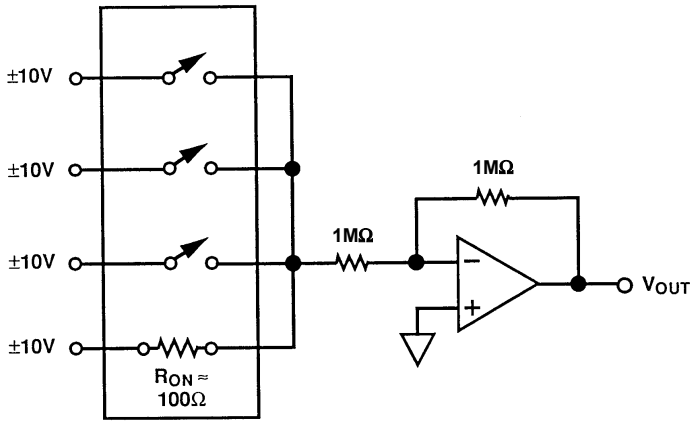
- **Switch drives a virtual ground.**
- **Switch sees only ±100mV, not ±10V, minimizes ΔR_{ON} .**

Figure 7.76: *Applying the Analog Switch: Minimizing the Influence of ΔR_{ON}*

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer, because any capacitance added to that node introduces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance, C_1, across the feedback resistor may be required to stabilize the circuit.

The finite value of R_{ON} can be a significant error source in the circuit shown in Figure 7.77. The gain-setting resistors should be at least 1,000 times larger than the switch on-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy but lower bandwidth and greater sensitivity to leakage and bias current.

A better method of compensating for R_{ON} is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 7.78. It is a safe assumption that the multiple switches, fabricated on a single chip, are well-matched in absolute characteristics and tracking over temperature. Therefore, the amplifier is closed-loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.



- **ΔR_{ON} is small compared to 1MΩ switch load.**
- **Effect on transfer accuracy is minimized.**
- **Bias current and leakage current effects are now very important.**
- **Circuit bandwidth degrades.**

Figure 7.77: *Applying the Analog Switch: Minimizing Effects of ΔR_{ON} Using Large Resistor Values*

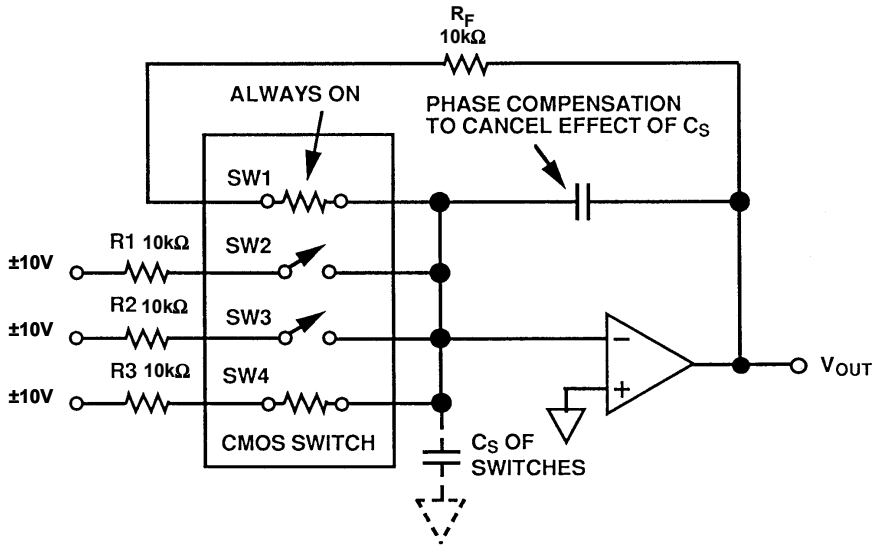


Figure 7.78: *Applying the Analog Switch:Using "Dummy" Switch in Feedback to Minimize Gain Error Due to ΔR_{ON}*

The best multiplexer design drives the non-inverting input of the amplifier as shown in Figure 7.79. The high input impedance of the non-inverting input eliminates the errors due to R_{ON}.

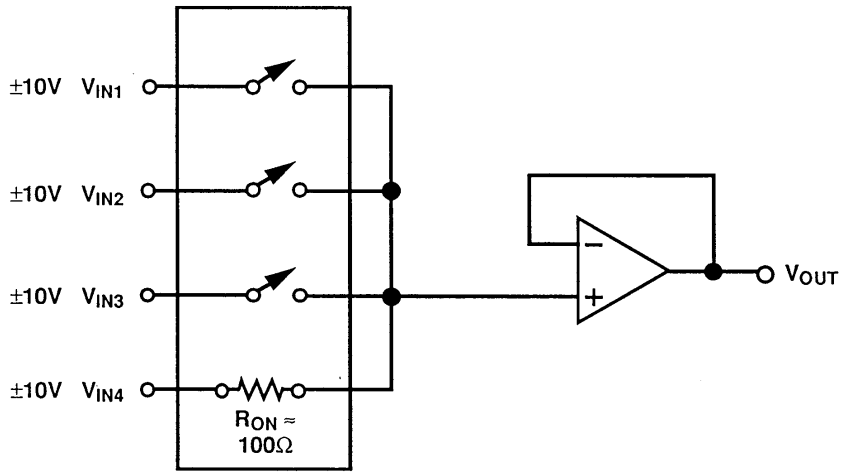
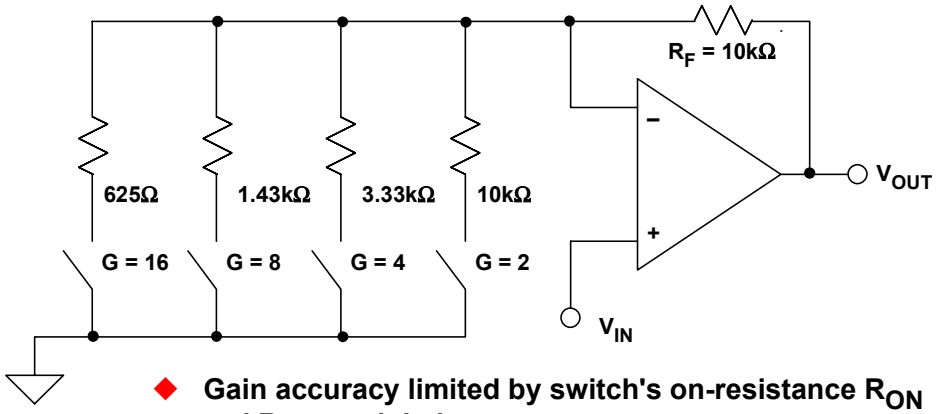


Figure 7.79: *Applying the Analog Switch: Minimizing the Influence of ΔR_{ON} Using Non-Inverting Configuration*

CMOS switches and multiplexers are often used with op amps to make programmable gain amplifiers (PGAs). To understand R_{ON}'s effect on their performance, consider Figure 7.80, a poor PGA design. A non-inverting op amp has 4 different gain-set resistors, each grounded by a switch, with an R_{ON} of 100-500 Ω. Even with R_{ON} as low as 25 Ω, the gain of 16 error would be 2.4%, worse than 8-bit accuracy! R_{ON} also changes over temperature, and from switch-to-switch.

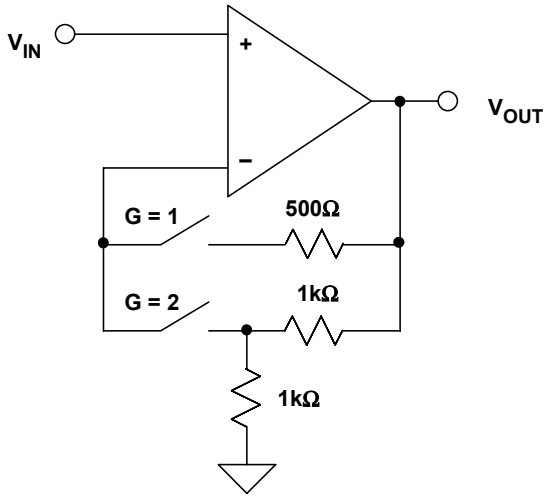


- **Gain accuracy limited by switch's on-resistance R_{ON} and R_{ON} modulation**
- **R_{ON} typically 1 - 500Ω for CMOS or JFET switch**
- **For R_{ON} = 25Ω, there is a 2.4% gain error for G = 16**
- **R_{ON} drift over temperature limits accuracy**
- **Must use very low R_{ON} switches**

Figure 7.80: *A Poorly Designed PGA Using CMOS Switches*

To attempt "fixing" this design, the resistors might be increased, but noise and offset could then be a problem. The only way to improve accuracy with this circuit is to use relays, with virtually no R_{ON}. Only then will the few mΩ of relay R_{ON} be a small error vis-à-vis 625 Ω.

It is much better to use a circuit insensitive to R_{ON}! In Figure 7.81, the switch is placed in series with the inverting input of an op amp. Since the op amp input impedance is very large, the switch R_{ON} is now irrelevant, and gain is now determined solely by the external resistors. Note—R_{ON} may add a small offset error if op amp bias current is high. If this is the case, it can readily be compensated with an equivalent resistance at V_{IN}.



- **R_{ON} is not in series with gain setting resistors**
- **R_{ON} is small compared to input impedance**
- **Only slight offset errors occur due to bias current flowing through the switches**

Figure 7.81: *Alternate PGA Configuration Minimizes the Effects of R_{ON}*

1-GHz CMOS Switches

The ADG918/ADG919 are the first switches using a CMOS process to provide high isolation and low insertion loss up to and exceeding 1 GHz. The switches exhibit low insertion loss (0.8 dB) and relatively high off isolation (37 dB) when transmitting a 1-GHz signal. In high frequency applications with throughput power of +18 dBm or less at 25°C, they are a cost-effective alternative to gallium arsenide (GaAs) switches. A block diagram of the devices are shown in Figure 7.82 along with isolation and loss versus frequency plots given in Figure 7.83.

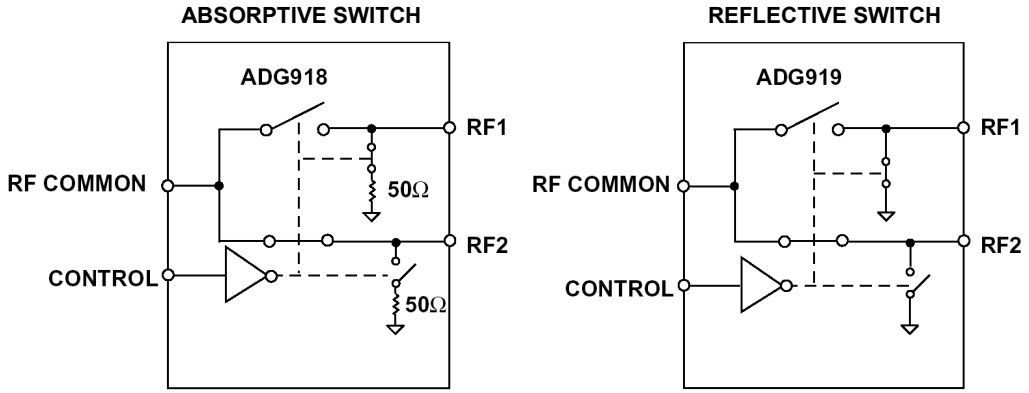


Figure 7.82: *1-GHz CMOS 1.65-V to 2.75-V 2:1 Mux/SPDT Switches*

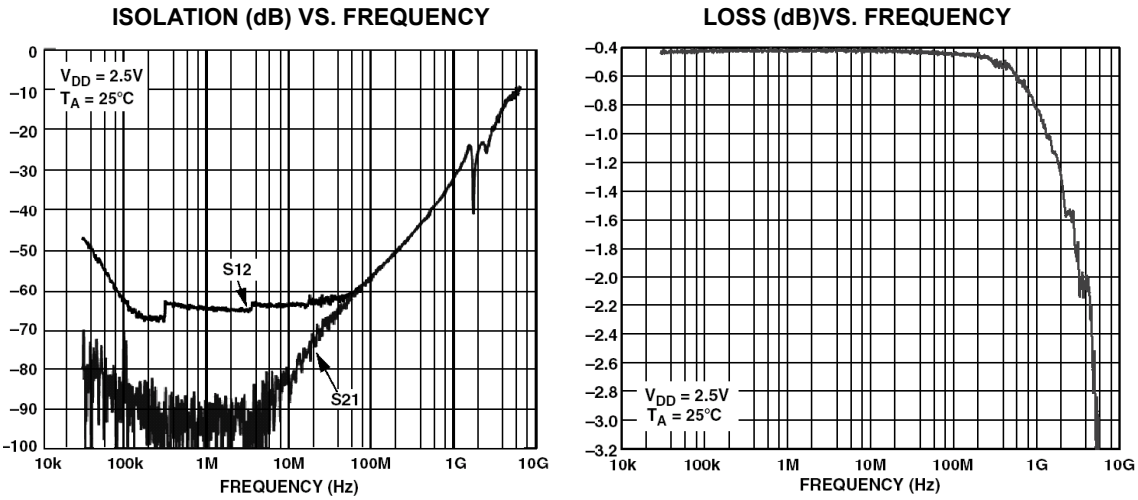


Figure 7.83: *Isolation and Frequency Response of AD918/AD919 1-GHz Switch*

The ADG918 is an absorptive switch with 50-Ω terminated shunt legs that allow impedance matching with the application circuit, while the ADG919 is a reflective switch designed for use where the terminations are external to the chip. Both offer low power consumption (<1 μA), tiny packages (8-lead MSOP and 3 mm × 3 mm lead frame chip scale package), single-pin control voltage levels that are CMOS/LVTTL compatible, making the switches ideal for wireless applications and general-purpose RF switching.

Video Switches and Multiplexers

In order to meet stringent specifications of bandwidth flatness, differential gain and phase, and 75-Ω drive capability, high speed complementary bipolar processes are more suitable than CMOS processes for video switches and multiplexers. Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 50 ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch on-resistance with signal level (R_{on} *modulation*) introduces unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies. The tradeoffs, of course, are higher power and cost.

Functional block diagrams of the AD8170/8174/8180/8182 bipolar video multiplexer are shown in Figure 7.84. The AD8183/AD8185 video multiplexer is shown in Figure 7.85. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10ns to 0.1%. The AD8186/8187 are single-supply versions of the AD8183/8185. Note that these bipolar multiplexers are not bi-directional.

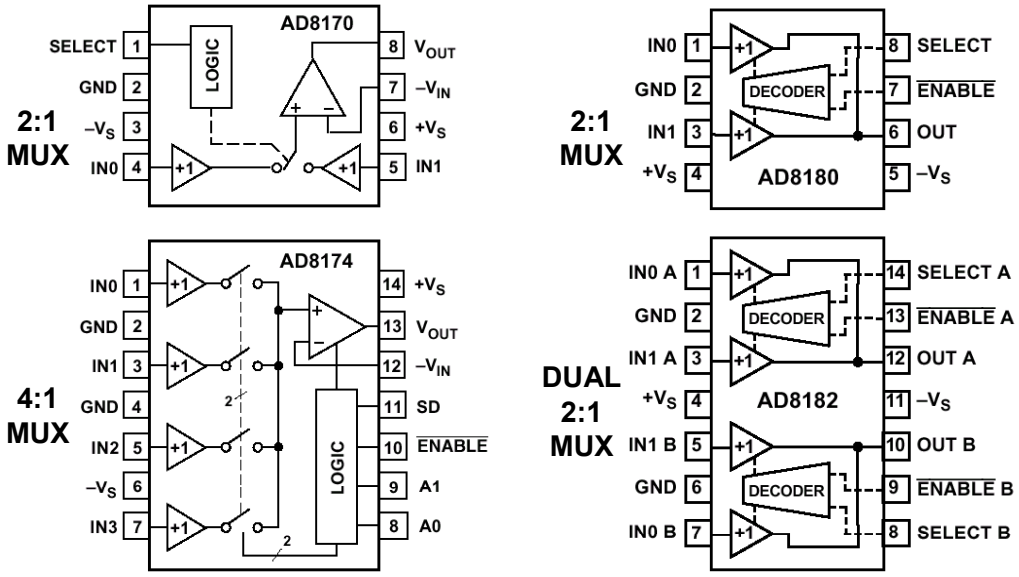


Figure 7.84: *AD8170/8174/8180/8182 Bipolar Video Multiplexers*

The AD8170/8174 series of muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80 dB at 5 MHz for the entire family.

Figure 7.86 shows an application circuit for three AD8170 2:1 muxes, where a single RGB monitor is switched between two RGB computer video sources.

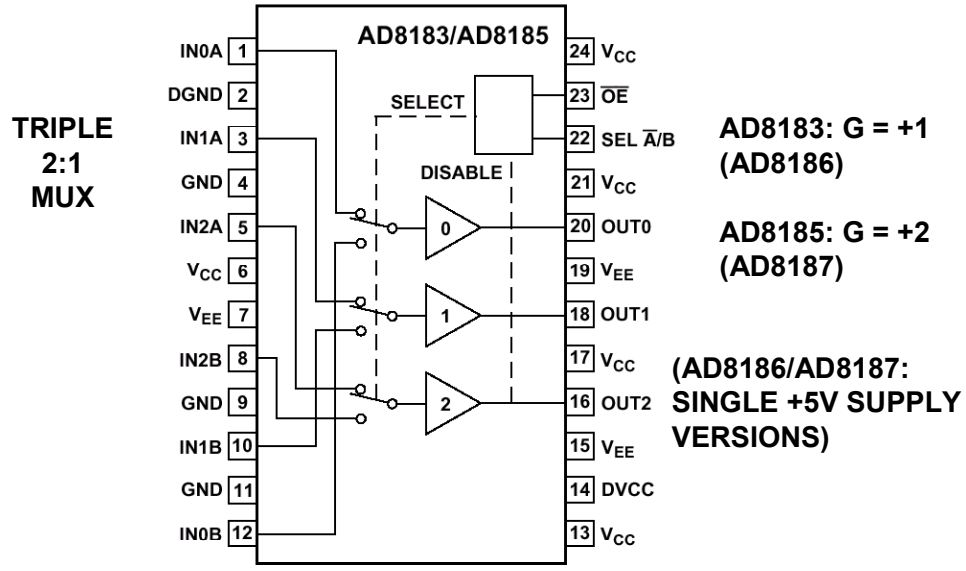


Figure 7.85: *AD8183/AD8185 Triple 2:1 Video Multiplexers*

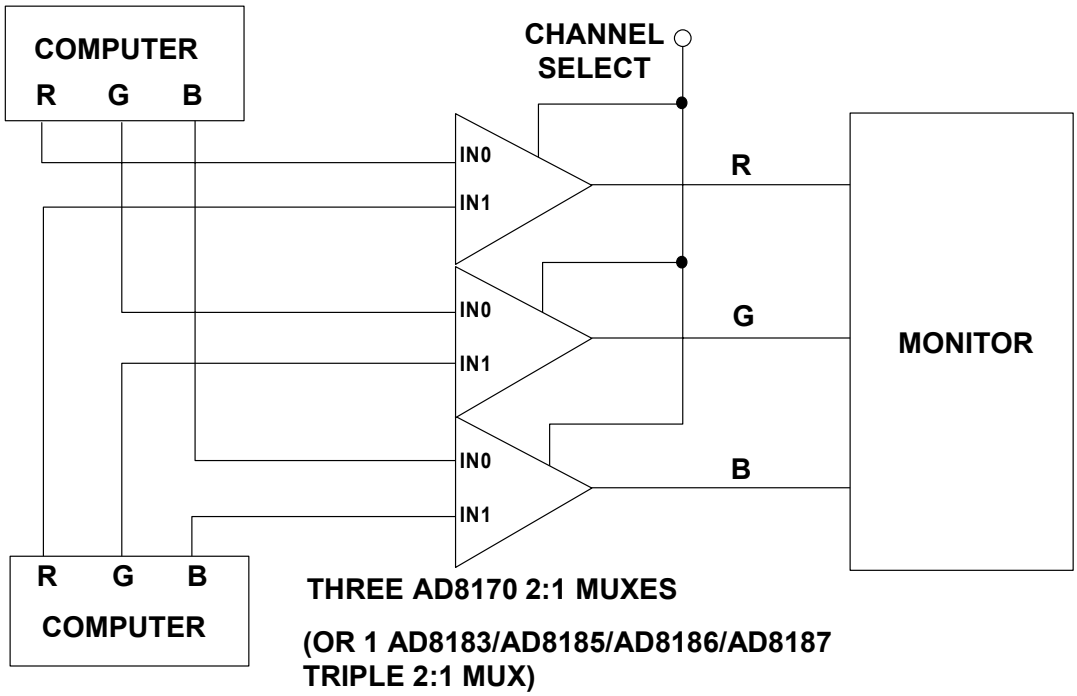


Figure 7.86: *Dual Source RGB Multiplexer Using Three 2:1 Muxes*

In this setup, the overall effect is that of a three-pole, double-throw switch. The three video sources constitute the three poles, and either the upper or lower of the video sources constitute the two switch states. Note that the circuit can be simplified by using a single AD8183, AD8185, AD8186, or AD8187 triple dual input multiplexer.

The AD8174 or AD8184 4:1 mux is used in Figure 7.87, to allow a single high speed ADC to digitize the RGB outputs of a scanner.

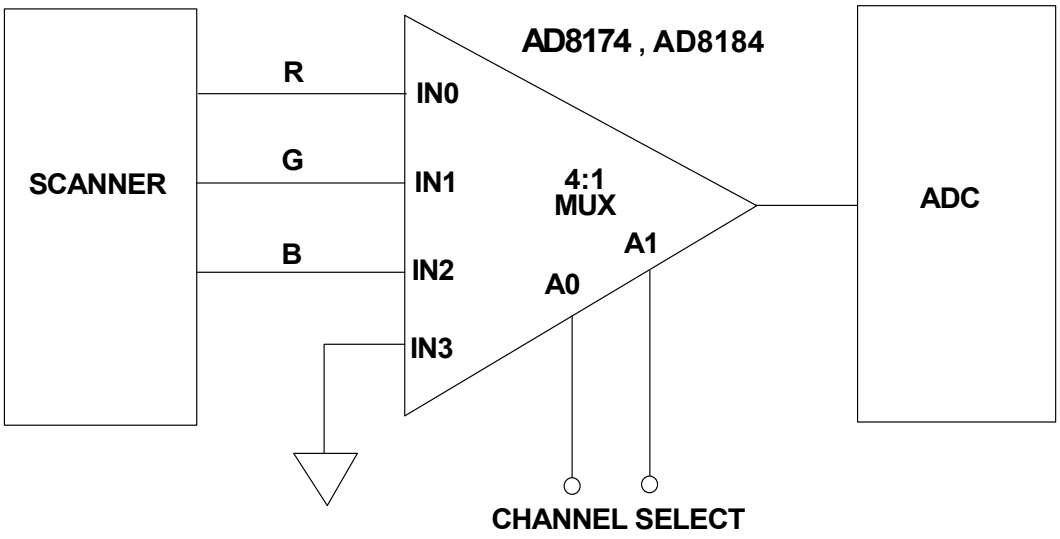


Figure 7.87: *Digitizing RGB Signals with One ADC and a 4:1 Mux*

The RGB video signals from the scanner are fed in sequence to the ADC, and digitized in sequence, making efficient use of the scanner data with one ADC.

Video Crosspoint Switches

The AD8116 extends the multiplexer concepts to a fully integrated, 16×16 buffered video crosspoint switch matrix (Figure 7.88). The 3-dB bandwidth is greater than 200 MHz, and the 0.1-dB gain flatness extends to 60 MHz. Channel switching time is less than 30 ns to 0.1%. Channel-to-channel crosstalk is −70 dB measured at 5 MHz. Differential gain and phase is 0.01% and 0.01° for a 150-Ω load. Total power dissipation is 900 mW on ±5 V.

The AD8116 includes output buffers that can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control that can accommodate "daisy chaining" of several devices. The AD8116 package is a 128-pin 14 mm × 14 mm LQFP. Other members of the crosspoint switch family include the AD8108/AD9109 8 × 8 crosspoint switch; the AD8110/AD8111, 260-MHz, 16 × 8, buffered crosspoint switch; the AD8113 audio/video 60-MHz, 16 × 16 crosspoint switch; and the AD8114/AD8115 low cost 225-MHz, 16 × 16, crosspoint switch.

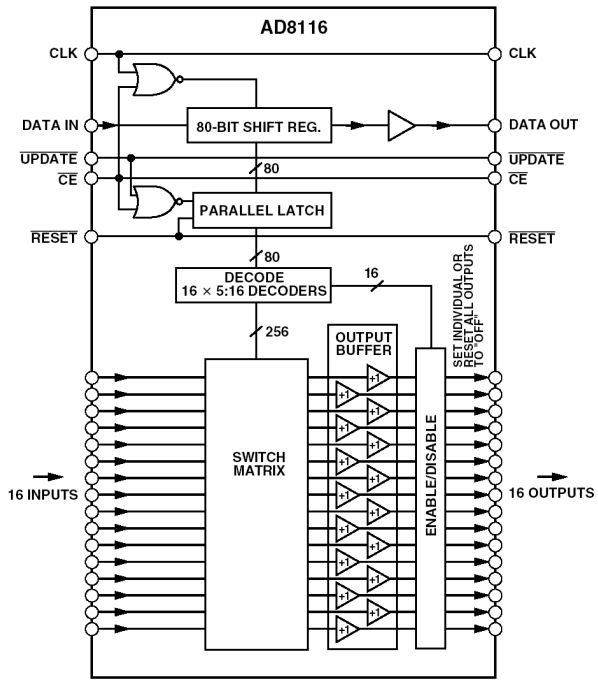


Figure 7.88: *AD8116 16×16 200-MHz Buffered Video Crosspoint Switch*

Digital Crosspoint Switches

The AD8152 is a 3.2-Gbps 34 × 34 asynchronous digital crosspoint switch designed for high speed networking (see Figure 7.89). The device operates at data rates up to 3.2 Gbps per port, making it suitable for Sonet/SDH OC-48 with Forward Error Correction (FEC). The AD8152 has digitally programmable current mode outputs that can drive a variety of termination schemes and impedances while maintaining the correct voltage level and minimizing power consumption. The part operates with a supply voltage as low as +2.5 V, with excellent input sensitivity. The control interface is compatible with LVTTL or CMOS/TTL.

As the lowest power solution of any comparable crosspoint switch, the AD8152 dissipates less than 2 W at 2.5-V supply with all I/Os active and does not require external heat sinks. The low jitter specification of less than 45 ps makes the AD8152 ideal for high speed networking systems. The AD8152's fully differential signal path reduces jitter and crosstalk while allowing the use of smaller single-ended voltage swings. It is offered in a 256-ball SBGA package that operates over the industrial temperature range of 0°C to +85°C.

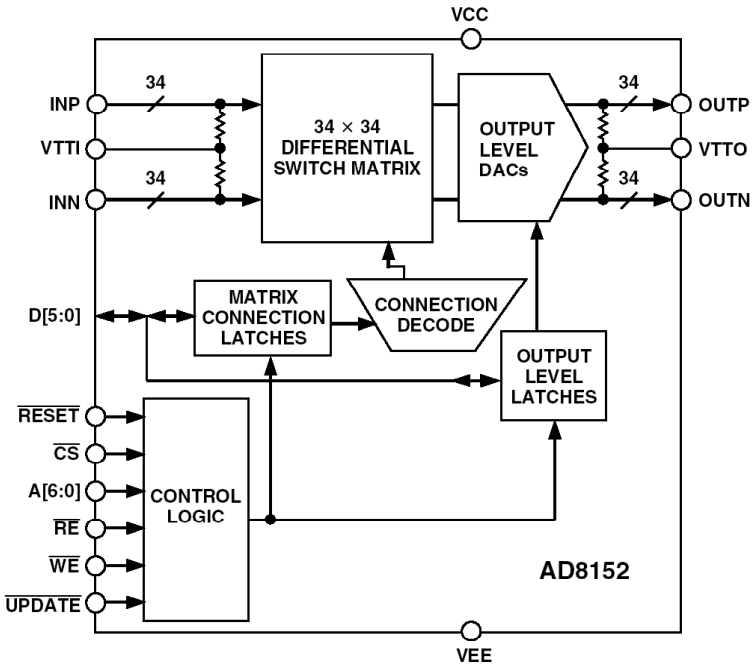


Figure 7.89: *AD8152 3.2-Gbps Asynchronous Digital Crosspoint Switch*

Switch and Multiplexer Families from Analog Devices

Selecting the right switch or multiplexer for a particular application can be a difficult task in light of the large number of devices currently offered. Selection guides from Analog Devices can be invaluable in this process. Figure 7.90 summarizes the generic families of CMOS switches and multiplexers, starting with the higher voltage devices and working downward to the newer lower voltage parts. While certainly not all-inclusive, this listing can be useful in getting an overall idea of available choices. Figure 7.91 summarizes the bipolar switch and multiplexer families. The ADG32xx-series of Bus Switches are discussed in more detail in Chapter 9.

- ADG2xx, ADG4xx, ADG5xx: ±15V
- ADG508F, ADG509F, ADG528F, ADG438F, ADG439F: Fault-protected ±15V family
- ADG12xx: ±15V, Low R_{ON} (2Ω)
- ADG14xx: ±15V , Low C_{ON} (2pF)
- ADG6xx: Single +5V (some lower) or ±5V
  - 3Ω R_{ON} family
  - 1pC charge injection family
  - 125°C family
- ADG7xx: Single +5V (some as low as +1.8V)
  - Some as low as 2.5Ω R_{ON}
  - Some in CSP
  - 3-5pC charge injection
- ADG8xx: Single +1.8V to +5.5V
  - <0.5Ω R_{ON}
- ADG9xx: Single +1.65V to +2.75V, > 1 GHz RF switches
- ADG3xxx: Bus Switches and Logic Level Shifters

Figure 7.90: *CMOS Switches and Multiplexer Families from Analog Devices*

- Video switches and multiplexers:
  - AD8074, AD8075, AD8170, AD8174, AD8180, AD8182, AD8184, AD8185, AD8186, AD8187
- Video crosspoint switches:
  - AD8108, AD8109, AD8110, AD8111, AD8114, AD8115, AD8116
- Audio and Video crosspoint switch:
  - AD8113
- Digital crosspoint switches:
  - AD8150, AD8151, AD8152, ADSX34

Figure 7.91: *High-Speed Bipolar Switches and Multiplexers from ADI*

Parasitic Latchup in CMOS Switches and Muxes

Because multiplexers are often at the front-end of a data acquisition system, their inputs generally come from remote locations—hence, they are often subjected to overvoltage conditions. Although this topic is treated in more detail in Chapter 9, an understanding of the problem as it relates to CMOS devices is particularly important. Although this discussion centers around multiplexers, it is germane to nearly all types of CMOS parts.

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 7.92. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than V_{DD} or more negative than V_{SS}. Even a transient situation, such as power-on with an input voltage present, can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

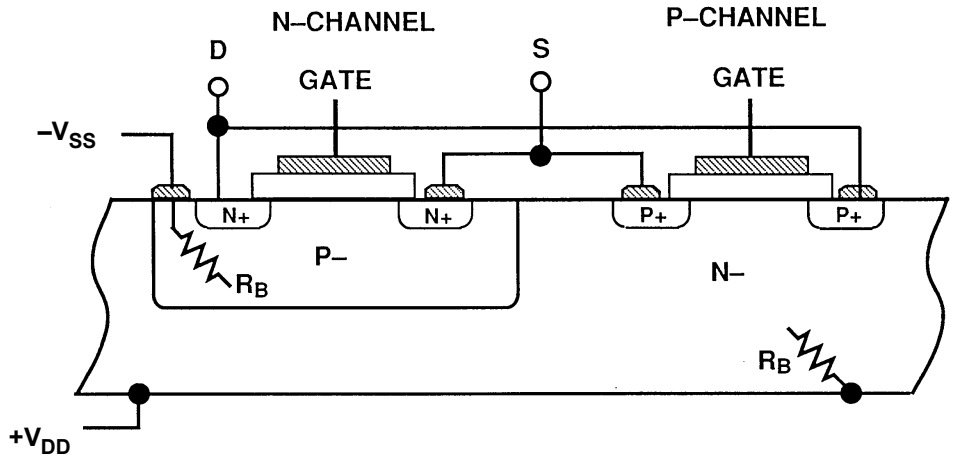


Figure 7.92: *Cross-Section of a Junction-Isolation CMOS Switch*

The parasitic SCR mechanism is shown in Figure 7.93. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than V_{DD} or one diode drop more negative than V_{SS}. In the former case, the V_{DD} terminal becomes the SCR gate input and provides the current to trigger SCR action. In the case where the voltage is more negative than V_{SS}, the V_{SS} terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

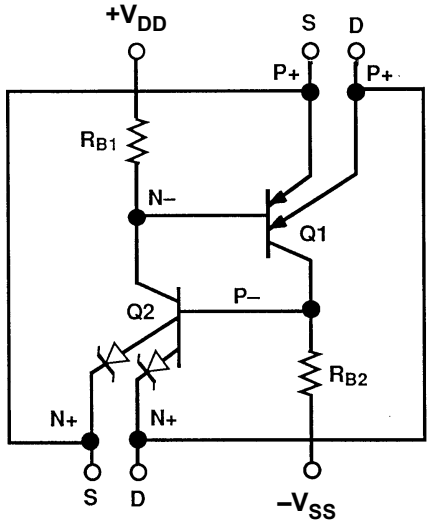
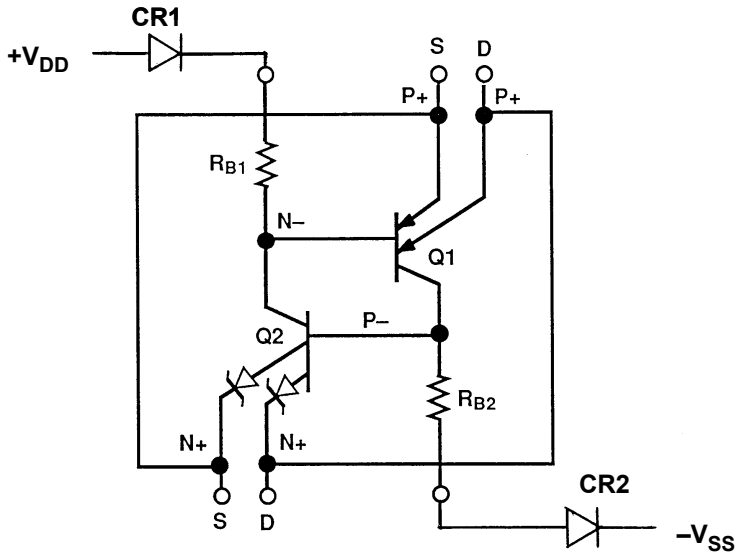


Figure 7.93: *Bipolar Transistor Equivalent Circuit for CMOS Switch Shows Parasitic SCR Latch*

In general, to prevent the latchup condition, the inputs to CMOS devices should never be allowed to be more than 0.3 V above the positive supply or 0.3 V below the negative supply. Note that this restriction also applies when the power supplies are off (V_{DD} = V_{SS} = 0 V), and therefore devices can latchup if power is applied to a part when signals are present on the inputs. Manuracturers of CMOS devices invariably place this restriction in the data sheet table of absolute maximum ratings. In addition, the input current under overvoltage conditions should be restricted to 5-30 mA, depending upon the particular device.

In order to prevent this type of SCR latchup, a series diode can be inserted into the V_{DD} and V_{SS} terminals as shown in Figure 7.94. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.



Diodes CR1 and CR2 block base current drive to Q1 and Q2 in the event of overvoltage at S or D.

Figure 7.94: *Diode Protection Scheme for CMOS Switch*

If diode protection is used, the analog voltage range of the switch will be reduced by one V_{BE} drop at each rail, and this can be inconvenient when using low supply voltages.

As noted, CMOS switches and multiplexers can also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level as shown in Figure 7.95, generally less than 5-30 mA. Because of the resitive attenuator formed by R_{LOAD} and R_{LIMIT}, this method works only if the switch drives a relatively high impedance load.

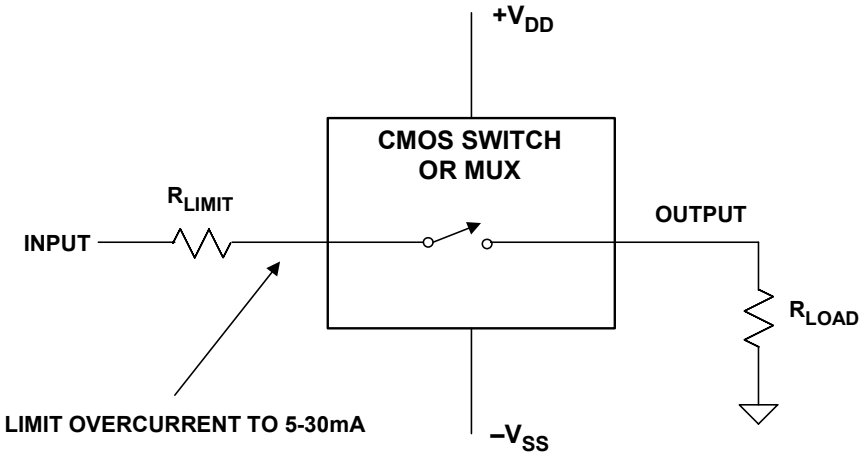


Figure 7.95: *Overcurrent Protection Using External Resistor*

A common method for input protection is shown in Figure 7.96 where Schottky diodes are connected from the input terminal to each supply voltage as shown. The diodes effectively prevent the inputs from exceeding the supply voltage by more than 0.3-0.4 V, thereby preventing latchup conditions. In addition, if the input voltage exceeds the supply voltage, the input current flows through the external diodes to the supplies, not the device. Schottky diodes can easily handle 50-100 mA of transient current, therefore the R_{LIMIT} resistor can be quite low.

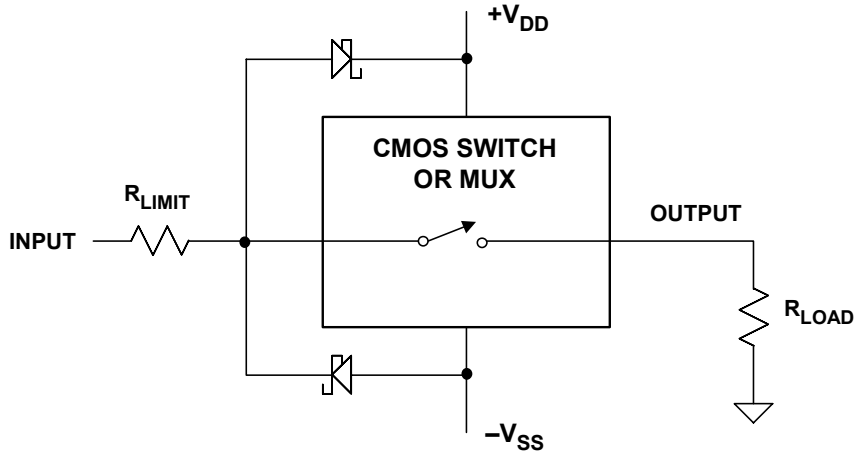


Figure 7.96: *Input Protection Using External Schottky Diodes*

Most CMOS devices have internal ESD-protection diodes connected from the inputs to the supply rails, making the devices less susceptible to latchup. However, the internal diodes begin conduction at 0.6 V, and have limited current-handling capability, thus adding the external Schottky diodes offers an added degree of protection. However, the effects of the diode leakage and capacitance must be considered.

Note that latchup protection does not provide overcurrent protection, and vice versa. If both fault conditions can exist in a system, then both protective diodes and resistors should be used.

Analog Devices uses trench-isolation technology to produce its LC^{2}MOS analog switches. The process reduces the latchup susceptibility of the device, the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

Figure 7.97 shows the cross-sectional view of the trench-isolated CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction. Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

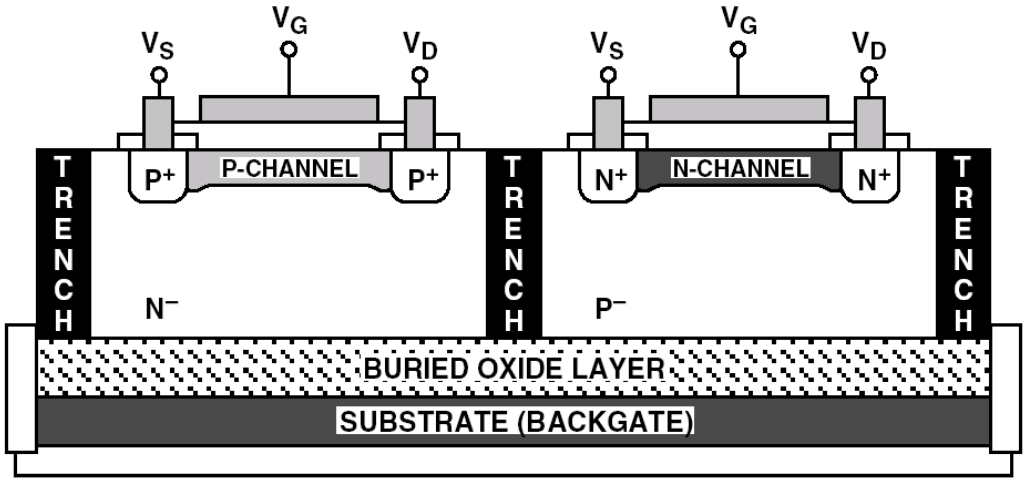


Figure 7.97: *Trench-Isolation LC^{2}MOS Structure*

The ADG508F, ADG509F, ADG528F, ADG438F, and ADG439F are ±15-V trench-isolated LC^{2}MOS multiplexers which offer "fault protection" for input and output overvoltages between –40 V and + 55 V. These devices use a series structure of three MOSFETS in the signal path: an N-channel, followed by a P-channel, followed by an N-channel. In addition, the signal path becomes a high impedance when the power supplies are turned off. This structure offers a high degree of latchup and overvoltage protection—at the expense of higher R_{ON} (~300 Ω), and more R_{ON} variation with signal level. For more details of this protection method, refer to the individual product data sheets.

NOTES:

SECTION 7.4: SAMPLE-AND-HOLD CIRCUITS

Walt Kester

Introduction and Historical Perspective

The *sample-and-hold amplifier*, or SHA, is a critical part of most data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

When the SHA is used with an ADC (either externally or internally), the SHA performance is critical to the overall dynamic performance of the combination, and plays a major role in determining the SFDR, SNR, etc., of the system.

Although today the SHA function has become an integral part of the *sampling* ADC, understanding the fundamental concepts governing its operation is essential to understanding ADC dynamic performance.

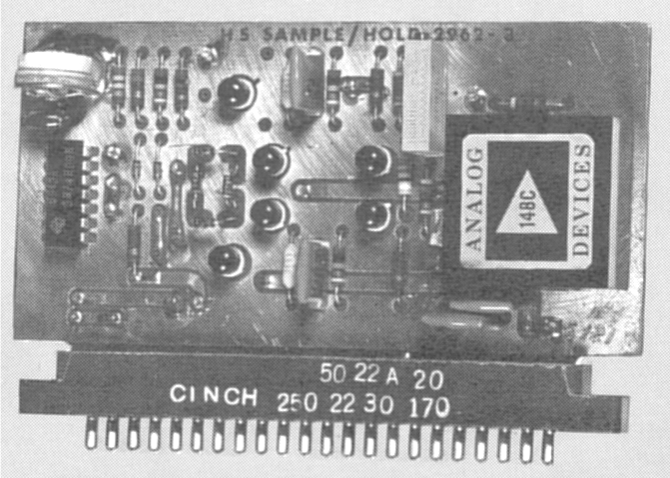
When the sample-and-hold is in the sample (or track) mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period (such as the AD684, AD781, and AD783). These will not be considered here. Strictly speaking, a sample-and-hold with good tracking performance should be referred to as a *track-and-hold* circuit, but in practice the terms are used interchangeably.

The most common application of a SHA is to maintain the input to an ADC at a constant value during conversion. With many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted—this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion.

From a historial perspective, it is interesting that the ADC described by A. H. Reeves in his famous PCM patent of 1939 (Reference 1) was a 5-bit 6-kSPS counting ADC where the analog input signal drove a vacuum tube pulse-width-modulator (PWM) directly—the sampling function was incorporated into the PWM. Subsequent work on PCM at Bell Labs led to the use of electron-beam encoder tubes and successive approximation ADCs; and Reference 2 (1948) describes a companion 50-kSPS vacuum tube sample-and-hold circuit based on a pulse transformer drive circuit.

There was increased interest in sample-and-hold circuits for ADCs during the period of the late 1950s and early 1960s as transistors replaced vacuum tubes. One of the first analytical treatments of the errors produced by a solid-state sample-and-hold was published in 1964 by Gray and Kitsopolos of Bell Labs (Reference 3). Edson and Henning of Bell Labs describe the results of experimental work done on a 224-Mbps PCM system, including the 9-bit ADC and a companion 12-MSPS sample-and-hold. References 4, 5 , and 6 are representative of work done on sample-and-hold circuits during the 1960s and early 1970s.

In 1969, the newly acquired Pastoriza division of Analog Devices offered one of the first commercial sample-and-holds, the SHA1 and SHA2 as shown in Figure 7.98. The circuits were offered on PC boards, and the SHA1 had an acquisition time of 2 µs to 0.01%, dissipated 0.9 W, and cost approximately $225. The faster SHA2 had an acquisition time of 200 ns to 0.01%, dissipated 1.7 W, and cost approximately $400. They were designed to operate with 12-bit successive approximation ADCs also offered on PC boards.



- **Acquisition Time: 2µs to 0.01% (SHA1), 200ns to 0.01% (SHA2)**
- **Power: 900mW (SHA1), 1.7W (SHA2)**
- **$225 (SHA1), $400 (SHA2)**

Figure 7.98: *"SHA1 and SHA2" Sample-and-Holds from Analog Devices' Pastoriza Division, 1969*

Modular and hybrid technology quickly made the PC board sample-and-holds obsolete, and the demand for sample-and-holds increased as IC ADCs, such as the industry-standard AD574, came on the market. In the 1970s and into the 1980s, it was quite common for system designers to purchase separate sample-and-holds to drive such ADCs, because process technology did not allow integrating them together onto the same chip. IC SHAs such as the AD582 (4-µs acquisition time to 0.01%), AD583 (6-µs acquisition time to 0.01%), and the AD585 (3-µs acquisition time to 14-bit accuracy) served the lower speed markets of the 1970s and 1980s.

Hybrid SHAs such as the HTS-0025 (25-ns acquisition time to 0.1%), HTC-0300 (200-ns acquisition time to 0.01%), and the AD386 (25-µs acquisition time to 16-bits) served the high-speed, high-end markets. By 1995, Analog Devices offered approximately 20 sample-and-hold products for various applications, including the following high-speed ICs: AD9100/AD9101 (10-ns acquisition time to 0.01%), AD684 (quad 1-µs acquisition time to 0.01%) and the AD783 (250-ns acquisition time to 0.01%).

However, ADC technology was rapidly expanding during the same period, and many ADCs were being offered with internal SHAs (i.e., *sampling* ADCs). This made them easier to specify and certainly easier to use. Integration of the SHA function was made

possible by new process developments including high-speed complementary bipolar processes and advanced CMOS processes. In fact, the proliferation and popularity of sampling ADCs has been so great that today (2003), one rarely has the need for a separate SHA.

The advantage of a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall dc and ac performance is fully specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA. This is especially important when one considers dynamic specifications such as SFDR and SNR.

Although the largest applications of SHAs are with ADCs, they are also occasionally used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

Basic SHA Operation

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 7.99.

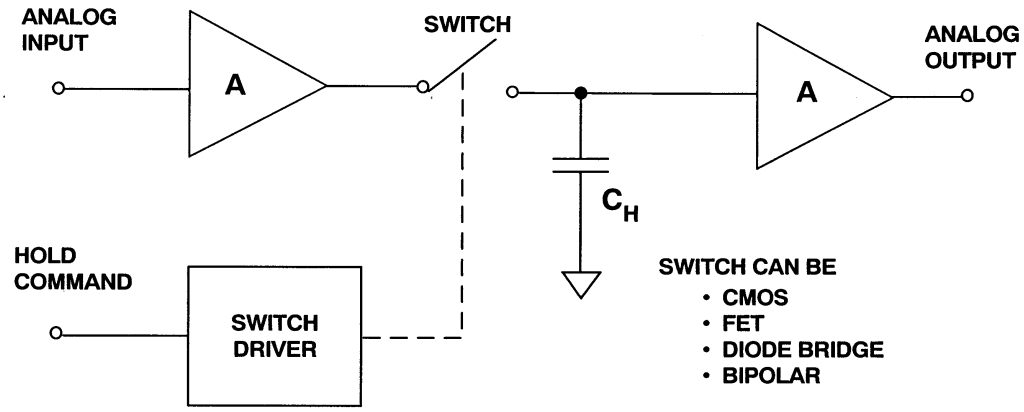


Figure 7.99: *Basic Sample-and-Hold Circuit*

The energy-storage device, the heart of the SHA, is a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the *track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 7.100, and some of the SHA error sources are shown graphically in Figure 7.101. Because there are both dc and ac performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
STATIC: ◆ Offset ◆ Gain Error ◆ Nonlinearity	STATIC: ◆ Pedestal ◆ Pedestal Nonlinearity	STATIC: ◆ Droop ◆ Dielectric ◆ Absorption	
DYNAMIC: ◆ Settling Time ◆ Bandwidth ◆ Slew Rate ◆ Distortion ◆ Noise	DYNAMIC: ◆ Aperture Delay Time ◆ Aperture Jitter ◆ Switching Transient ◆ Settling Time	DYNAMIC: ◆ Feedthrough ◆ Distortion ◆ Noise	DYNAMIC: ◆ Acquisition Time ◆ Switching Transient

Figure 7.100: *Sample-and-Hold Specifications*

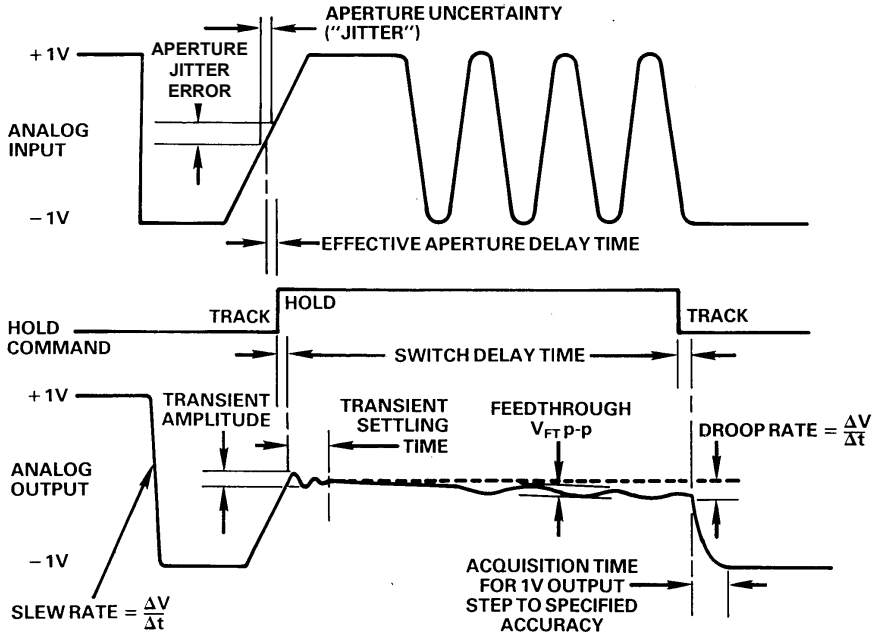


Figure 7.101: *Some Sources of Sample-and-Hold Errors*

Track Mode Specifications

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold mode.) The principle track mode specifications are *offset*, *gain*, *nonlinearity*, *bandwidth*,

slew rate, *settling time*, *distortion*, and *noise*. However, distortion and noise in the track mode are often of less interest than in the hold mode.

Track-to-Hold Mode Specifications

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of non-ideal switches. This results in a hold mode dc offset voltage which is called *pedestal* error as shown in Figure 7.102. If the SHA is driving an ADC, the pedestal error appears as a dc offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold-mode distortion.

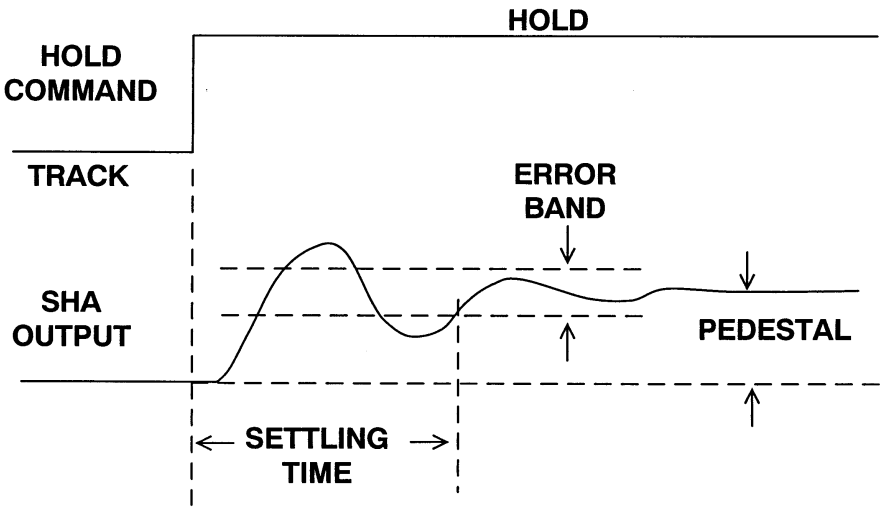


Figure 7.102: *Track-to-Hold Mode Pedestal, Transient, and Settling Time Errors*

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called *aperture time*. The various quantities associated with the internal SHA timing are shown in the Figure 7.103.

The actual value of the voltage that is held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself. Figure 7.104 shows what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold pedestal and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the

aperture time of the switch as shown in Figure 7.104. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance (t_a).

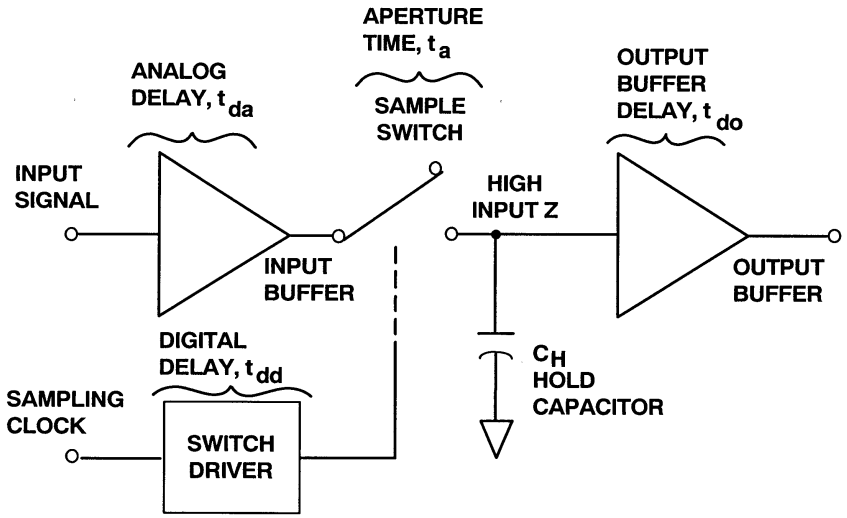


Figure 7.103: *SHA Circuit Showing Internal Timing*

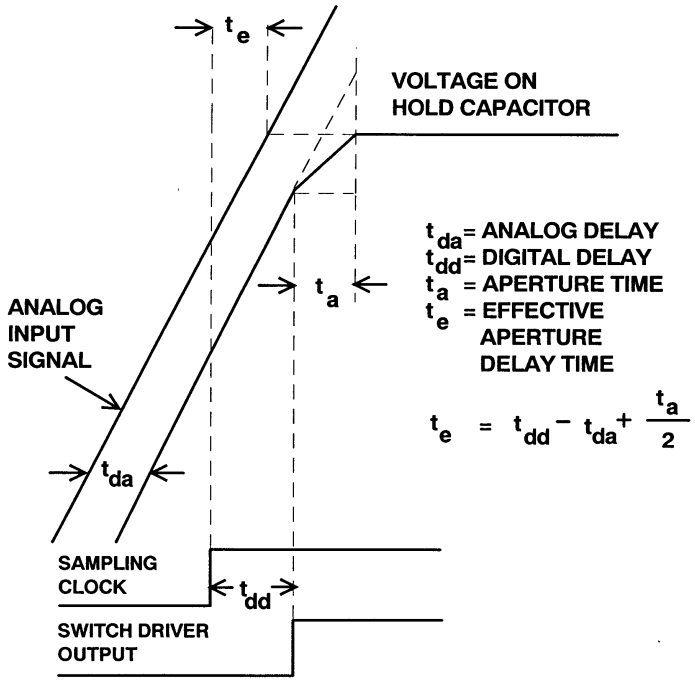


Figure 7.104: *SHA Waveforms*

The model shows that the finite time required for the switch to open (t_a) is equivalent to introducing a small delay in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. It is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, (t_e) and is defined as the time difference between

the analog propagation delay of the front-end buffer (t_{da}) and the switch digital delay (t_{dd}) plus one-half the aperture time ($t_a/2$). The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time ($t_a/2$) and the switch digital delay (t_{dd}) is less than the propagation delay through the input buffer (t_{da}). The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero-crossing of the input sinewave is the aperture delay time as shown in Figure 7.105.

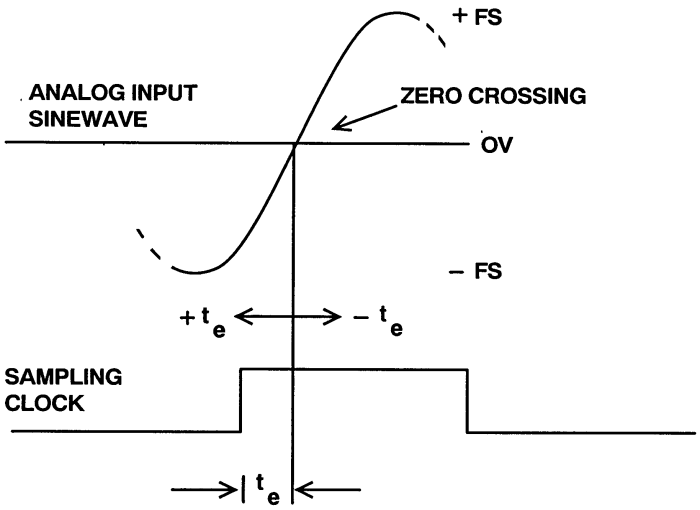


Figure 7.105: *Effective Aperture Delay Time*

Aperture delay produces no errors, but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). If there is sample-to-sample variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 7.106. This sample-to-sample variation in the instant the switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in picoseconds rms. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input dv/dt increases.

Measuring aperture jitter error in a SHA requires a jitter-free sampling clock and analog input signal source, because jitter (or phase noise) on either signal cannot be distinguished from the SHA aperture jitter itself—the effects are the same. In fact, the largest source of timing jitter errors in a system is most often external to the SHA (or the ADC if it is a sampling one) and is caused by noisy or unstable clocks, improper signal routing, and lack of attention to good grounding and decoupling techniques. SHA aperture jitter is generally less than 50-ps rms, and less than 5-ps rms in high speed devices. Details of measuring aperture jitter of an ADC can be found in Chapter 5.

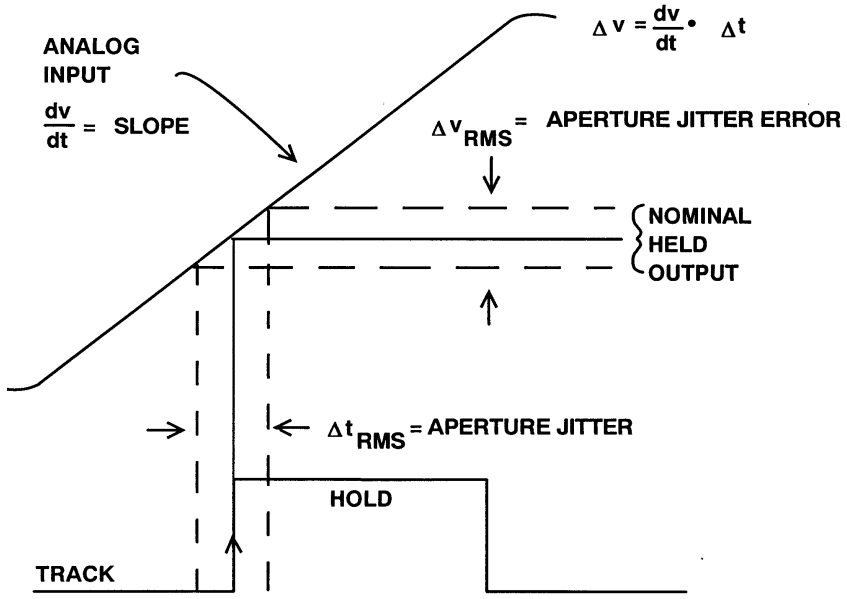


Figure 7.106: *Effects of Aperture or Sampling Clock Jitter on SHA Output*

Figure 7.107 shows the effects of total sampling clock jitter on the signal-to-noise ratio (SNR) of a sampled data system. The total rms jitter will be composed of a number of components, the actual SHA aperture jitter often being the least of them.

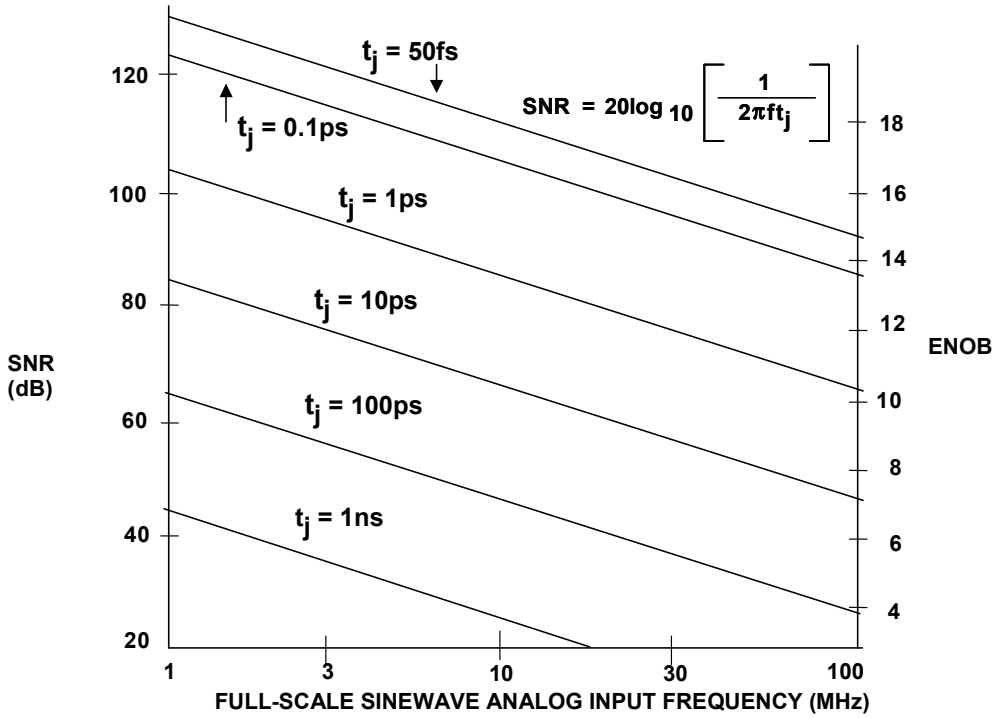


Figure 7.107: *Effects of Sampling Clock Jitter on SNR*

Hold Mode Specifications

During the hold mode there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows in or out of the hold capacitor, it will slowly charge or discharge, and its voltage will change. This effect is known as *droop* in the SHA output and is expressed in V/µs. Droop can be caused by leakage across a dirty PC board if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of the output buffer amplifier. An acceptable value of droop is where the output of a SHA does not change by more than ½ LSB during the conversion time of the ADC it is driving, although this value is highly dependent on the ADC architecture. Where droop is due to leakage current in reversed biased junctions (CMOS switches or FET amplifier gates), it will double for every 10°C increase in chip temperature—which means that it will increase a thousand fold between +25°C and +125°C. Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode. Differential techniques are often used to reduce the effects of droop in modern IC sample-and-hold circuits that are part of the ADC.

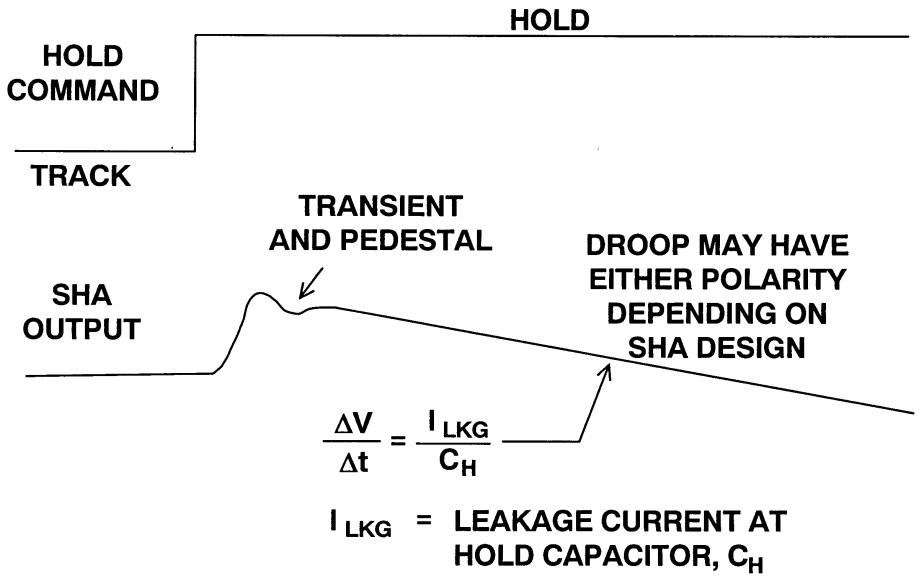
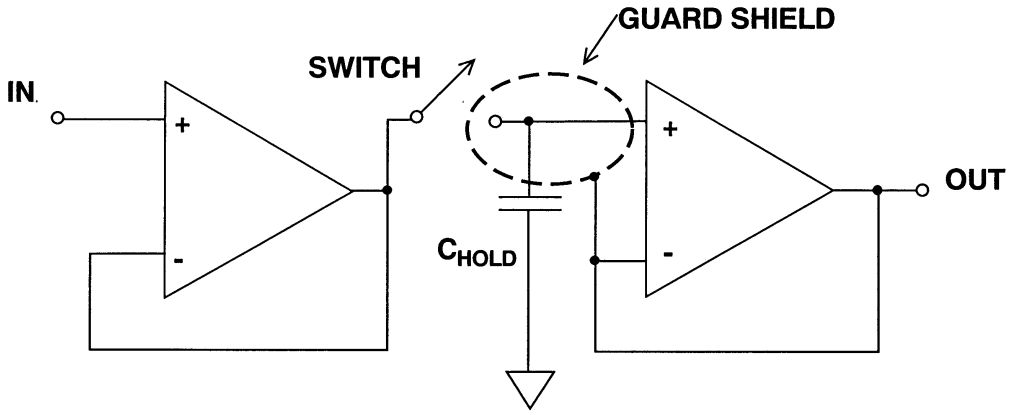


Figure 7.108: *Hold Mode Droop*

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them, there can be no leakage current flow. In a non-inverting application, such as is shown in Figure 7.109, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential (Figure 7.110). The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB—and on multi-layer boards, guard rings should be present in all layers.



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 7.109: *Drive the Guard Shield with the Same Voltage as the Hold Capacitor to Reduce Board Leakage*

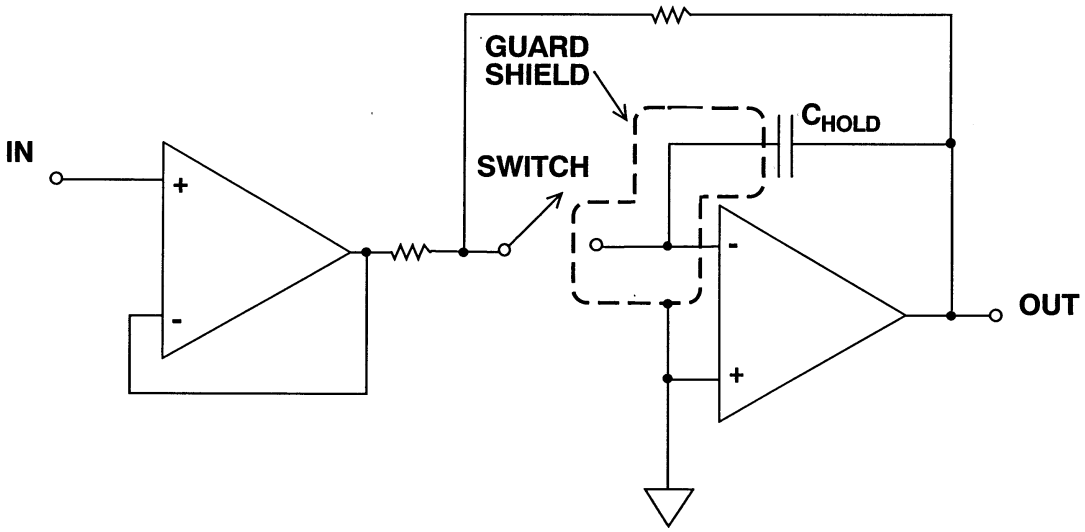


Figure 7.110: *Using a Guard Shield on a Virtual Ground SHA Design*

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit, it will recover some of its charge as shown in Figure 7.111. The phenomenon is known as *dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

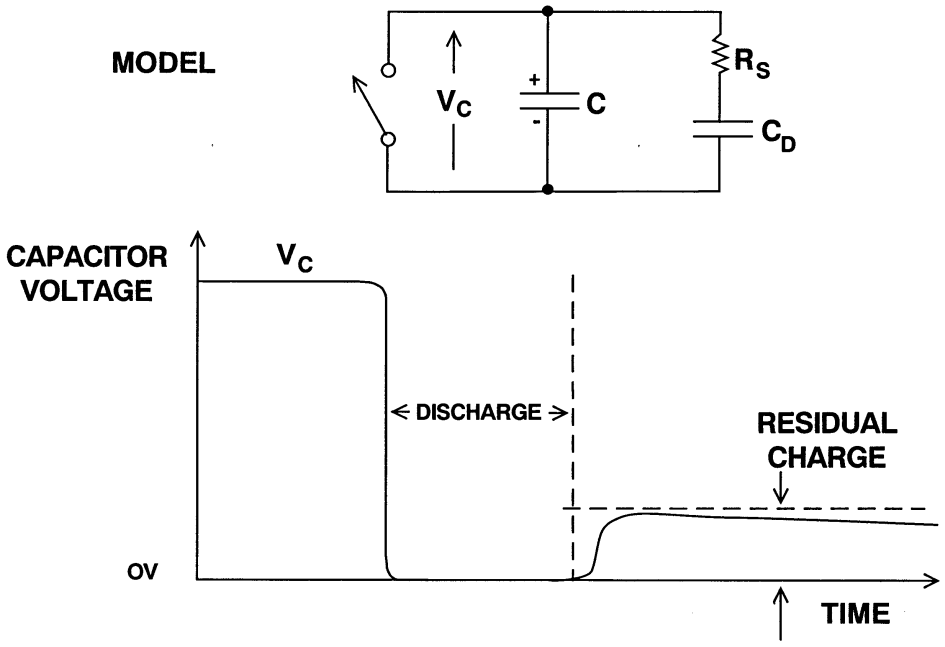


Figure 7.111: *Dielectric Absorption*

Different capacitor materials have differing amounts of dielectric absorption—electrolytic capacitors are dreadful (their leakage is also high), and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately, dielectric absorption varies from batch to batch, and even occasional batches of polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

Stray capacity in a SHA may allow a small amount of the ac input to be coupled to the output during hold. This effect is known as *feedthrough* and is dependent on input frequency and amplitude. If the amplitude of the feedthrough to the output of the SHA is more than ½ LSB, then the ADC is subject to conversion errors.

In many SHAs, distortion is specified only in the track mode. The *track mode distortion* is often much better than *hold mode distortion*. Track mode distortion does not include nonlinearities due to the switch network, and may not be indicative of the SHA performance when driving an ADC. Modern SHAs, especially high speed ones, specify distortion in both modes. While track mode distortion can be measured using an analog spectrum analyzer, hold mode distortion measurements should be performed using digital techniques as shown in Figure 7.112. A spectrally pure sinewave is applied to the SHA, and a low distortion high speed ADC digitizes the SHA output near the end of the hold time. An FFT analysis is performed on the ADC output, and the distortion components computed.

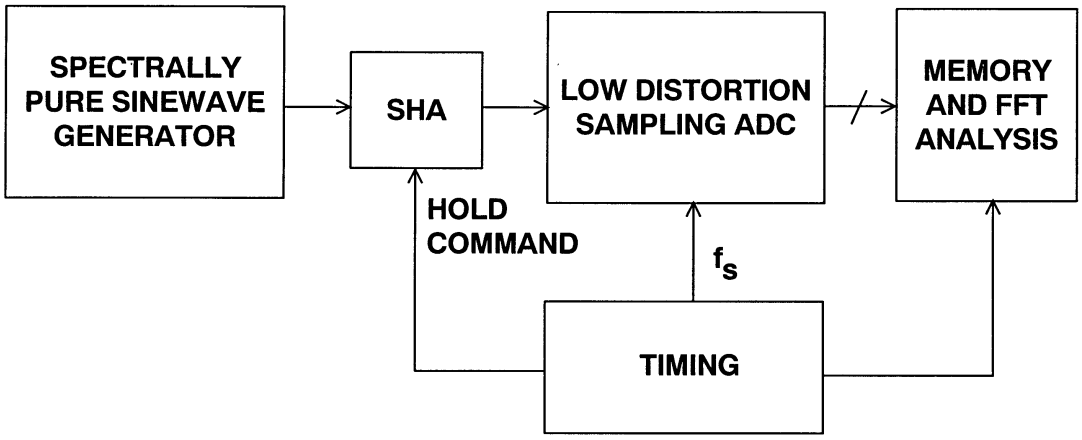


Figure 7.112: *Measuring Hold Mode Distortion*

SHA *noise* in the track mode is specified and measured like that of an amplifier. Peak-to-peak *hold mode noise* is measured with an oscilloscope and converted to an rms value by dividing by 6.6. Hold mode noise may be given as a spectral density in nV/√Hz, or as an rms value over a specified bandwidth. Unless otherwise indicated, the hold mode noise must be combined with the track mode noise to yield the total output noise. Some SHAs specify the total output hold mode noise, in which case the track mode noise is included.

Hold-to-Track Transition Specifications

When the SHA switches from hold to track, it must reacquire the input signal (which may have made a full scale transition during the hold mode). *Acquisition time* is the interval of time required for the SHA to reacquire the signal to the desired accuracy when switching from hold to track. The interval starts at the 50% point of the sampling clock edge, and ends when the SHA output voltage falls within the specified error band (usually 0.1% and 0.01% times are given). Some SHAs also specify acquisition time with respect to the voltage on the hold capacitor, neglecting the delay and settling time of the output buffer. The hold capacitor acquisition time specification is applicable in high speed applications, where the maximum possible time must be allocated for the hold mode. The output buffer settling time must of course be significantly smaller than the hold time.

Acquisition time can be measured directly using modern digital sampling scopes (DSOs) or digital phosphor scopes (DPOs) which are insensitive to large overdrives.

SHA Architectures

As with op amps, there are numerous SHA architectures, and we will examine a few of the most popular ones. The simplest SHA structure is shown in Figure 7.113. The input signal is buffered by an amplifier and applied to the switch. The input buffer may either be open- or closed-loop and may or may not provide gain. The switch can be CMOS, FET, or bipolar (using diodes or transistors) and is controlled by the switch driver circuit. The signal on the hold capacitor is buffered by an output amplifier. This architecture is sometimes referred to as *open-loop* because the switch is not inside a feedback loop.

Notice that the entire signal voltage is applied to the switch, therefore it must have excellent common-mode characteristics.

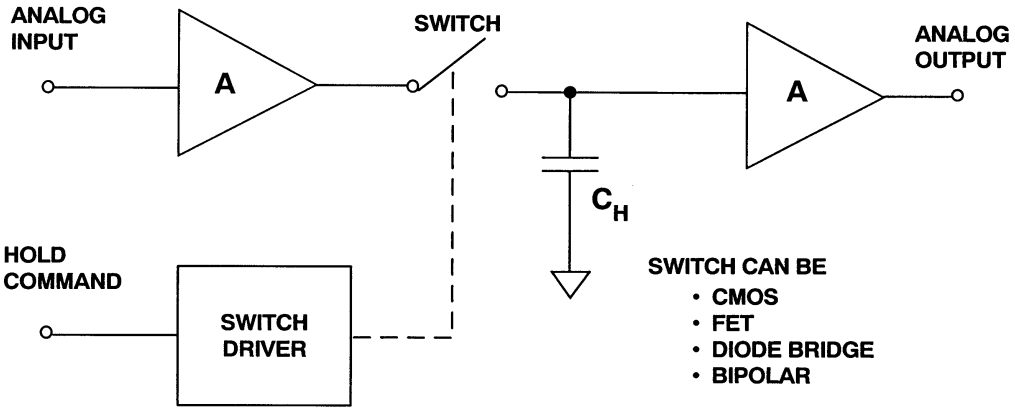


Figure 7.113: *Open-Loop SHA Architecture*

An implementation of this architecture is shown in Figure 7.114, where a simple diode bridge is used for the switch. In the track mode, current flows through the bridge diodes D1, D2, D3, and D4. For fast slewing input signals, the hold capacitor is charged and discharged with the current, I. Therefore, the maximum slew rate on the hold capacitor is equal to I/C_H. Reversing the bridge drive currents reverse biases the bridge and places the circuit in the hold mode. Bootstrapping the turn-off pulses with the held output signal minimizes common-mode distortion errors and is key to the circuit. The reverse bias bridge voltage is equal to the forward drops of D5 and D6 plus the voltage drops across the series resistors R1 and R2. This circuit is extremely fast, especially if the input and output buffers are open-loop followers, and the diodes are Schottky ones. The turn-off pulses can be generated with high frequency pulse transformers or with current switches as shown in Figure 7.115. This circuit can be used at any sampling rate, because the diode switching pulses are direct-coupled to the bridge. Variations of this circuit have been used since the mid 1960s in high speed PC board, modular, hybrid, and IC SHAs.

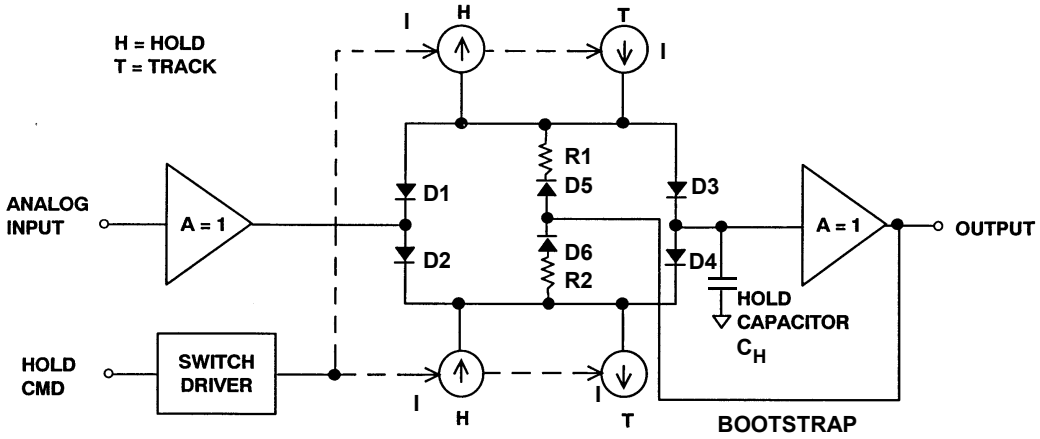


Figure 7.114: *Open-Loop SHA Using Diode Bridge Switch*

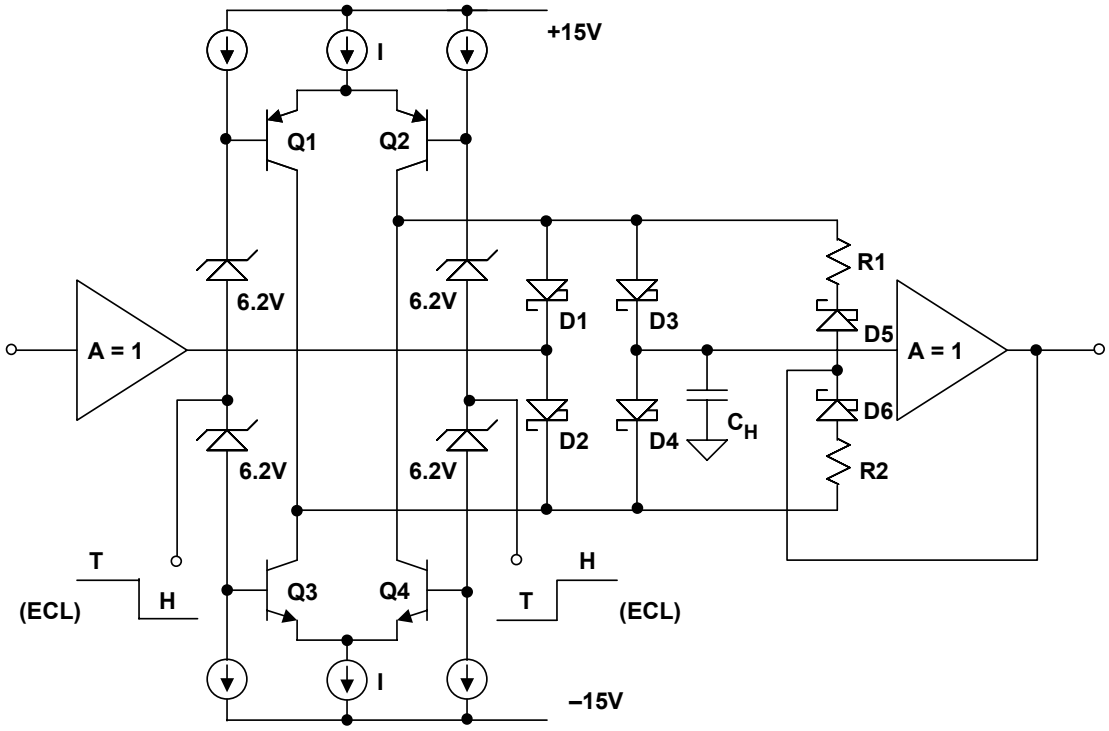


Figure 7.115: *Open-Loop SHA Implementation*

The SHA circuit shown in Figure 7.116 represents a classical *closed-loop* design and is used in many CMOS sampling ADCs. Since the switches always operate at virtual ground, there is no common-mode signal across them.

Switch S2 is required in order to maintain a constant input impedance and prevent the input signal from coupling to the output during the hold time. In the track mode, the transfer characteristic of the SHA is determined by the op amp, and the switches do not introduce dc errors because they are inside the feedback loop. The effects of charge injection can be minimized by using the differential switching techniques shown in Figure 7.117.

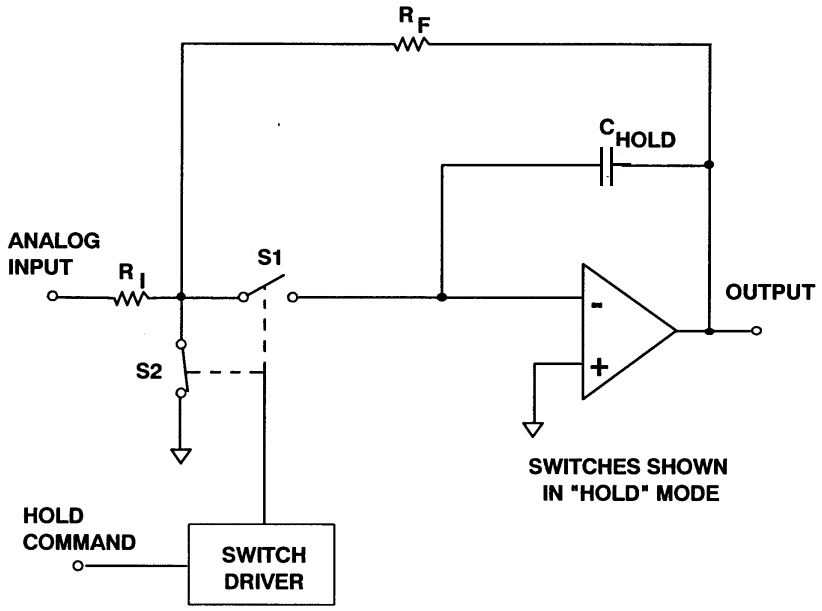


Figure 7.116: *Closed-Loop SHA Based on Inverting Integrator Switched at the Summing Point*

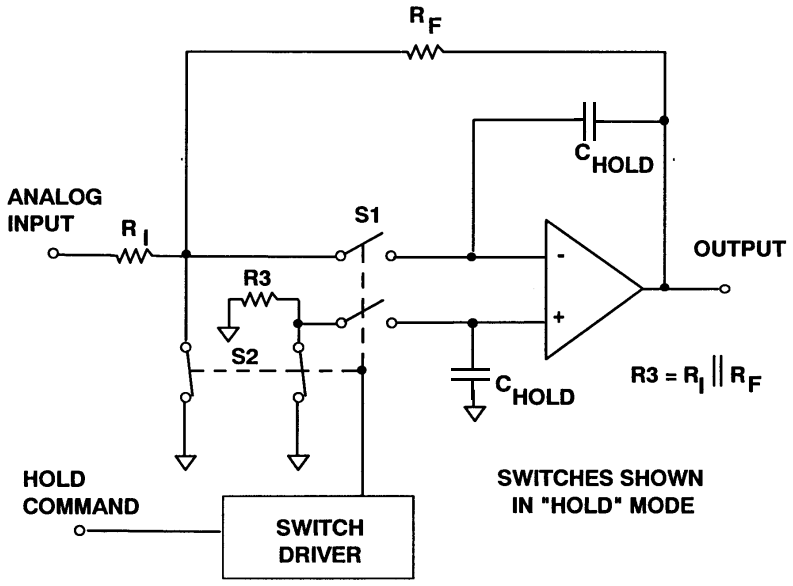


Figure 7.117: *Differential Switching Reduces Charge Injection*

Internal SHA Circuits for IC ADCs

CMOS ADCs are quite popular because of their low power and low cost. The equivalent input circuit of a typical CMOS ADC using a differential sample-and-hold is shown in Figure 7.118. While the switches are shown in the *track* mode, note that they open/close at the sampling frequency. The 16-pF capacitors represent the effective capacitance of switches S1 and S2, plus the stray input capacitance. The C_S capacitors (4 pF) are the

sampling capacitors, and the C_H capacitors are the hold capacitors. Although the input circuit is completely differential, this ADC structure can be driven either single-ended or differentially. Optimum performance, however, is generally obtained using a differential transformer or differential op amp drive.

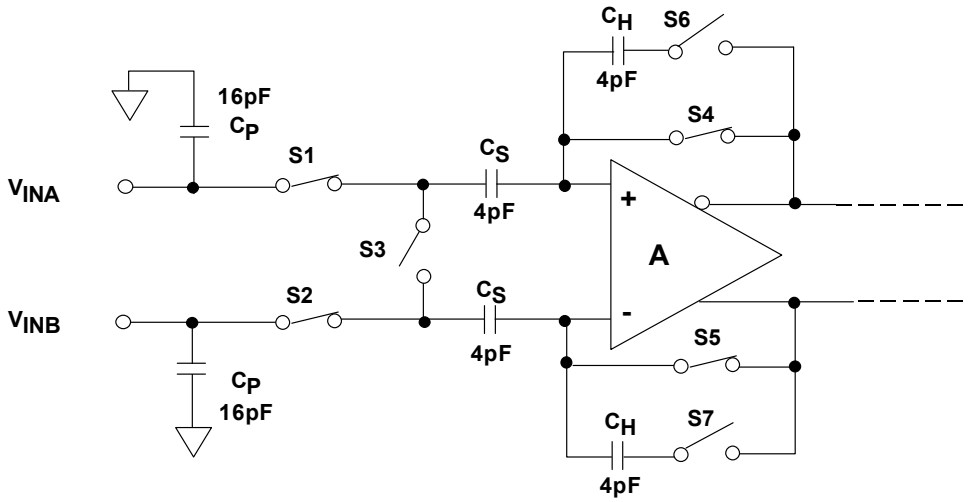


Figure 7.118: *Simplified Input Circuit for a Typical Switched Capacitor CMOS Sample-and-Hold*

In the *track* mode, the differential input voltage is applied to the C_S capacitors. When the circuit enters the *hold* mode, the voltage across the sampling capacitors is transferred to the C_H hold capacitors and buffered by the amplifier A (the switches are controlled by the appropriate sampling clock phases). When the SHA returns to the *track* mode, the input source must charge or discharge the voltage stored on C_S to a new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency f_S, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_S$), the input impedance is dynamic, and certain input drive source precautions should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that is drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a resistor equal to $1/(C_S f_S)$ connected between the inputs. Since C_S is only a few picofarads, this resistive component is typically greater than several kΩ for an f_S = 10 MSPS.

Figure 7.119 shows a simplified circuit of the input SHA used in the AD9042 12-bit, 41-MSPS ADC introduced in 1995 (Reference 7). The AD9042 is fabricated on a high speed complementary bipolar process, XFCB. The circuit comprises two independent SHAs in parallel for fully differential operation—only one-half the circuit is shown in the figure. Fully differential operation reduces the error due to droop rate and also reduces second-order distortion. In the track mode, transistors Q1 and Q2 provide unity-gain buffering. When the circuit is placed in the hold mode, the base voltage of Q2 is pulled negative until it is clamped by the diode, D1. The on-chip hold capacitor, C_H, is

nominally 6 pF. Q3 along with C_F provide output current bootstrapping and reduce the V_{BE} variations of Q2. This reduces third-order signal distortion. Track mode THD is typically –93 dB at 20 MHz. In the time domain, full-scale acquisition time to 12-bit accuracy is 8 ns. In the hold mode, signal-dependent pedestal variations are minimized by the voltage bootstrapping action of Q3 and the A = 1 buffer along with the low feedthrough parasitics of Q2. Hold mode settling time is 5 ns to 12-bit accuracy. Hold-mode THD at a clock rate of 50 MSPS and a 20-MHz input signal is –90 dB.

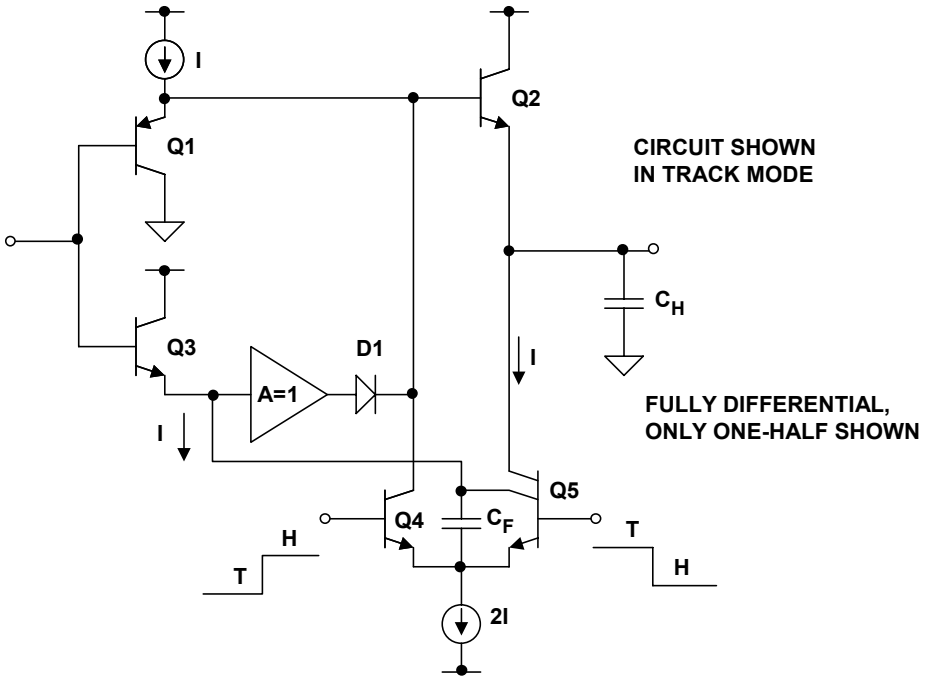


Figure 7.119: *SHA Used in AD9042 12-Bit, 41 MSPS ADC Introduced in 1995*

Figure 7.120 shows a simplified schematic of one-half of the differential SHA used in the AD6645 14-bit, 105-MSPS ADC recently introduced (Reference 9) gives a complete description of the ADC including the SHA). In the track mode, Q1, Q2, Q3, and Q4 form a complementary emitter follower buffer which drives the hold capacitor, C_H. In the hold mode, the polarity of the bases of Q3 and Q4 is reversed and clamped to a low impedance. This turns off Q1, Q2, Q3, and Q4, and results in double isolation between the signal at the input and the hold capacitor. As previously discussed, the clamping voltages are boostrapped by the held output voltage, thereby minimizing nonlinear effects.

Track mode linearity is largely determined by the V_{BE} modulation of Q3 and Q4 when charging C_H. Hold mode linearity depends on track mode linearity plus nonlinear errors in the track-to-hold transitions caused by imbalances in the switching of the base voltages of Q3 and Q4 and the resulting imbalance in charge injection through their base-emitter junctions as they turn off.

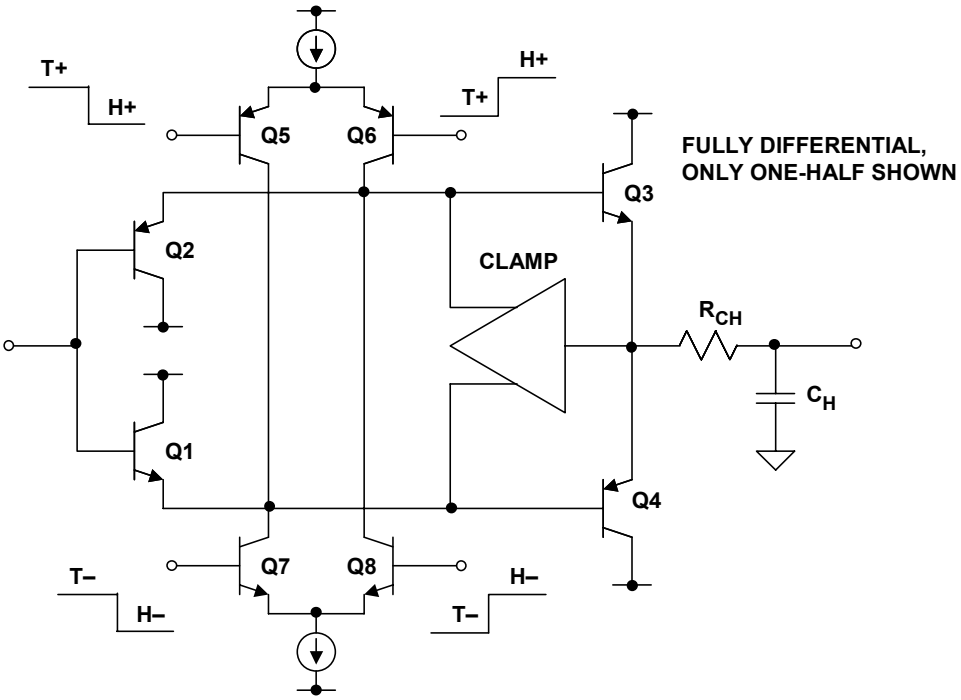


Figure 7.120: *SHA Used in AD6645 14-Bit, 105 MSPS ADC*

SHA Applications

By far the largest application of SHAs is driving ADCs. Most modern ADCs designed for signal processing are sampling ones and contain an internal SHA optimized for the converter design. Sampling ADCs are completely specified for both dc and ac performance and should be used in lieu of discrete SHA/ADC combinations wherever possible. In a very few selected cases, especially those requiring wide dynamic range and low distortion, there may be advantages to using a discrete combination.

A similar application uses a low distortion SHA to minimize the effects of code-dependent DAC glitches as shown in Figure 7.121. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are not code-dependent, occur at the update frequency, and are easily filterable. This technique may be useful at low frequencies to improve the distortion performance of DACs, but has little value when using high speed low-glitch low distortion DACs designed especially for DDS applications where the update rate is several hundred MHz.

Rather than use a single ADC per channel in a simultaneous sampled system, it is often more economical to use multiple SHAs followed by an analog multiplexer and a single ADC (Figure 7.122). Similarly, in data distribution systems multiple SHAs can be used to route the sequential outputs of a single DAC to multiple channels as shown in Figure 7.123; although this is not as common, as multiple DACs usually offer a better solution.

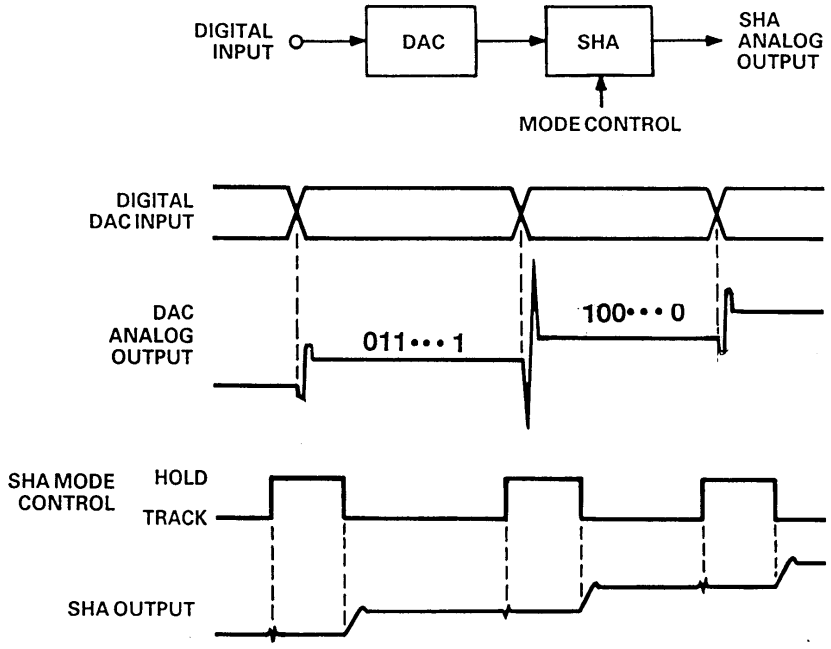


Figure 7.121: *Using a SHA as a DAC Deglitcher*

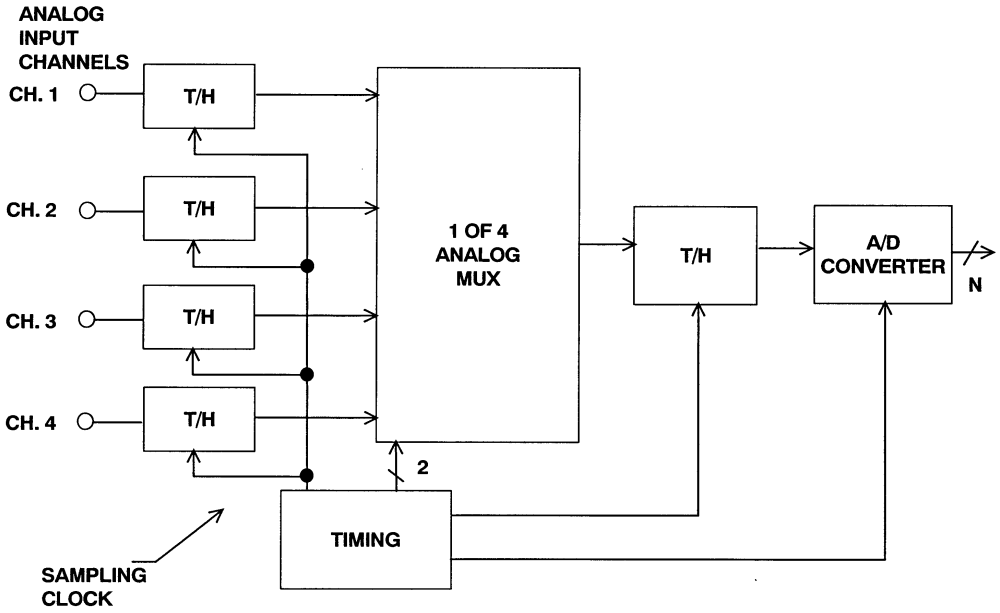


Figure 7.122: *Simultaneous Sampling Using Multiple SHAs and a Single ADC*

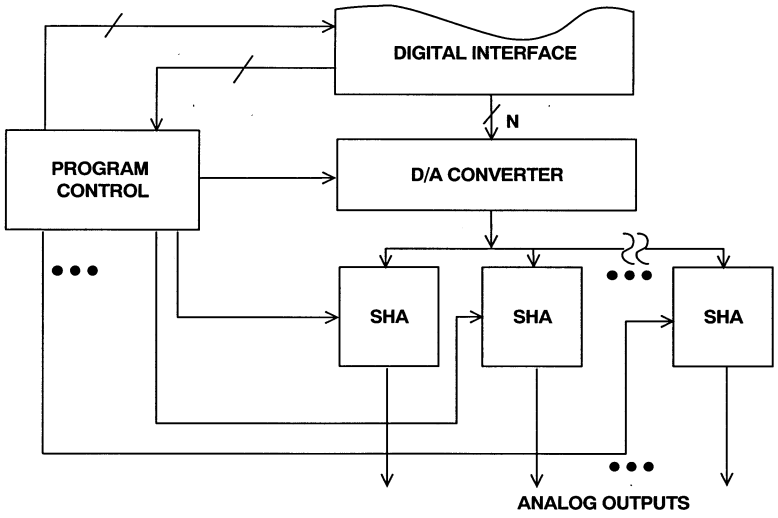


Figure 7.123: *Data Distribution System Using Multiple SHAs and a Single DAC*

A final application for SHAs is shown in Figure 7.124, where SHAs are cascaded to produce analog delay in a sampled data system. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a total pipeline delay greater than the sampling period T. This technique is often used in multi-stage pipelined subranging ADCs to allow for the conversion delays of successive stages. In pipelined ADCs, a 50% duty cycle sampling clock is common, thereby allowing alternating clock phases to drive each SHA in the pipeline (see Chapter 3 for more details of the pipelined ADC architecture and the use of SHAs for analog delay).

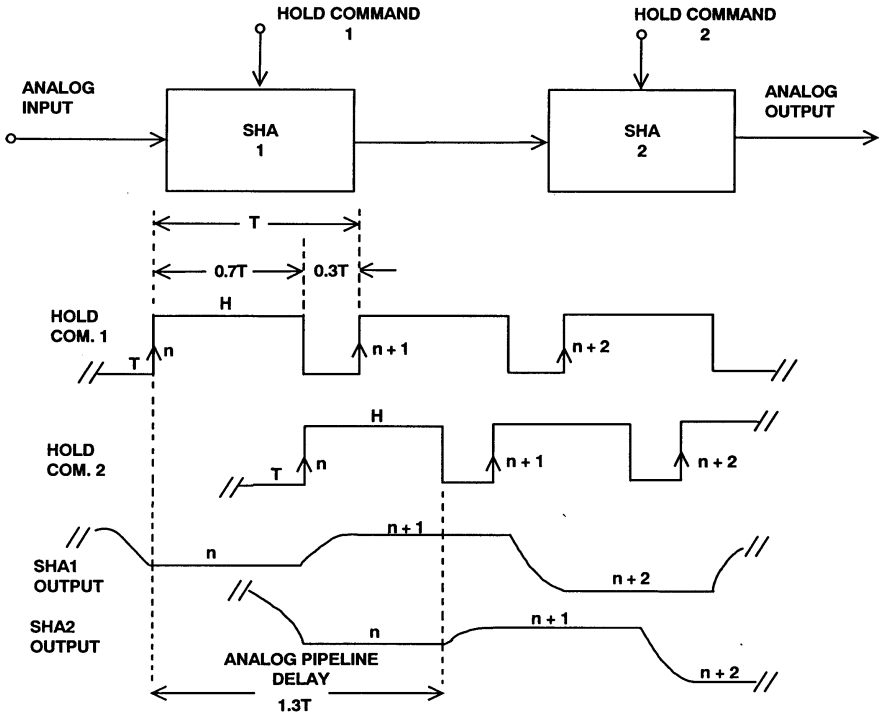


Figure 7.124: *SHAs Used for Analog Pipelined Delay*

REFERENCES:
7.4 SAMPLE-AND-HOLD CIRCUITS

1. Alec Harley Reeves, "Electric Signaling System," **U.S. Patent 2,272,070**, filed November 22, 1939, issued February 3, 1942. Also **French Patent 852,183** issued 1938, and **British Patent 538,860** issued 1939. *(the classic patents on PCM including descriptions of a 5-bit, 6-kSPS vacuum tube ADC and DAC).*

2. L. A. Meacham and E. Peterson, "An Experimental Multichannel Pulse Code Modulation System of Toll Quality," **Bell System Technical Journal**, Vol 27, No. 1, January 1948, pp. 1-43. *(describes the culmination of much work leading to this 24-channel experimental PCM system. In addition, the article describes a 50-kSPS vacuum tube sample-and-hold based on a pulse transformer driver).*

3. J. R. Gray and S. C. Kitsopoulos, "A Precision Sample-and-Hold Circuit with Subnanosecond Switching," **IEEE Transactions on Circuit Theory**, CT11, September 1964, pp. 389-396. *(an excellent description of a solid-state transformer-driven diode bridge SHA, along with a detailed mathematical analysis of the circuit and associated errors).*

4. J. O. Edson and H. H. Henning, "Broadband Codecs for an Experimental 224Mb/s PCM Terminal," **Bell System Technical Journal**, Vol. 44, pp. 1887-1940, Nov. 1965. *(summarizes experiments on ADCs based on the electron tube coder as well as a bit-per-stage Gray code 9-bit solid state ADC. The electron beam coder was 9-bits at 12MSPS, and represented the fastest of its type).*

5. D. J. Kinniment, D. Aspinall, and D.B.G. Edwards, "High-Speed Analogue-Digital Converter," **IEE Proceedings**, Vol. 113, pp. 2061-2069, Dec. 1966. *(a 7-bit 9MSPS three-stage pipelined error corrected converter is described based on recircuilating through a 3-bit stage three times. Tunnel (Esaki) diodes are used for the individual comparators. The article also shows a proposed faster pipelined 7-bit architecture using three individual 3-bit stages with error correction. The article also describes a fast bootstrapped transformer-driven diode-bridge sample-and-hold circuit).*

6. O. A. Horna, "A 150Mbps A/D and D/A Conversion System," **Comsat Technical Review**, Vol. 2, No. 1, pp. 39-72, 1972. *(a description of a subranging ADC including a detailed analysis of the sample-and-hold circuit).*

7. Roy Gosser and Frank Murden, "A 12-bit 50MSPS Two-Stage A/D Converter," **1995 ISSCC Digest of Technical Papers**, p. 278. *(a description of the AD9042 error corrected subranging ADC using MagAMP stages for the internal ADCs).*

8. Carl Moreland, "An 8-bit 150 MSPS Serial ADC," **1995 ISSCC Digest of Technical Papers**, Vol. 38, p. 272. *(a description of an 8-bit ADC with 5 folding stages followed by a 3-bit flash converter, including a discussion of the sample-and-hold circuit).*

9. Carl Moreland, Frank Murden, Michael Elliott, Joe Young, Mike Hensley, and Russell Stop, "A 14-bit 100-Msample/s Subranging ADC," **IEEE Journal of Solid State Circuits**, Vol. 35, No. 12, December 2000, pp. 1791-1798. *(describes the architecture used in the 14-bit, 105MSPS AD6645 ADC and also the sample-and-hold circuit).*

NOTES: